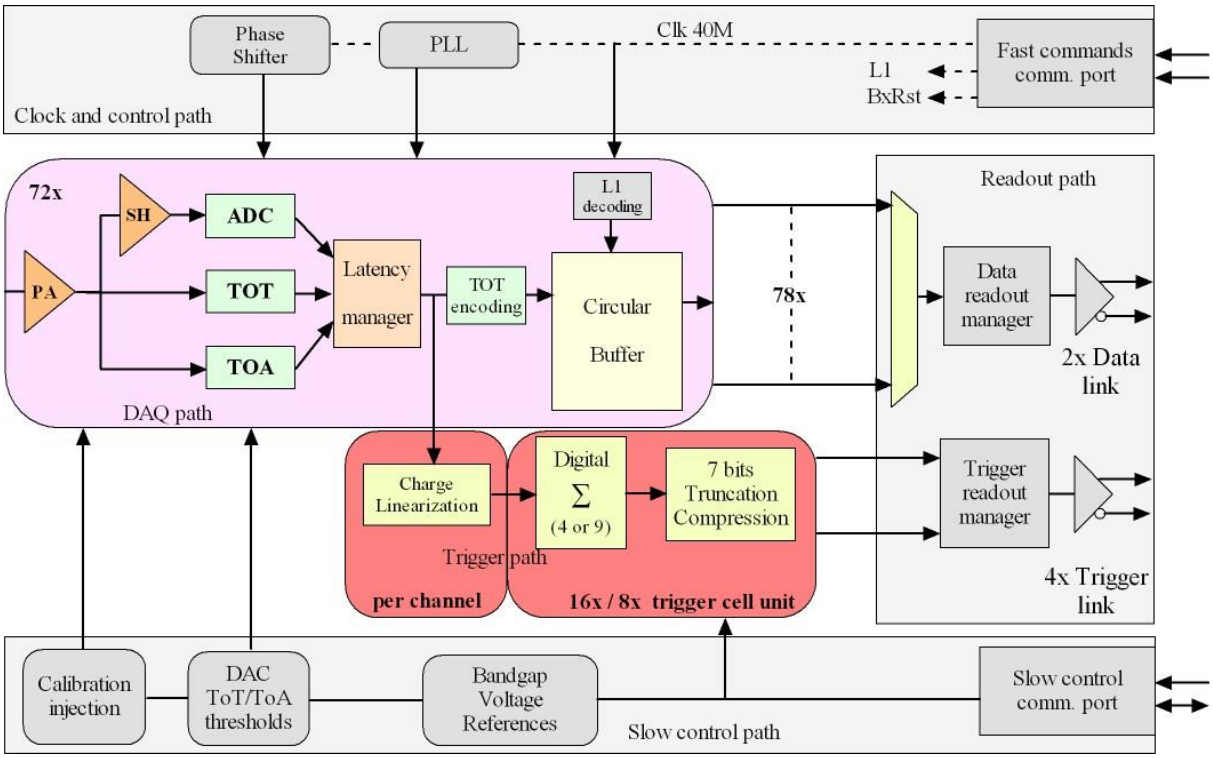
1 H2GCROC2/2A: architectural overview

The overall block diagram is described as per below. Compared to HGCROCV1, the “one channel” undergoes no functional change, as well as the trigger path. The memory is changed from SRAM to DRAM to save power and the electrical and physical interfaces are now be the final ones. An important modification is the final pinout, going from wire bonding to C4 bump bonding. The chip handles 72 channels + 4 channels for common mode subtraction + 2 special calibration channels.



1.1 Analog front-end

The front-end may be divided in three main sub-parts:

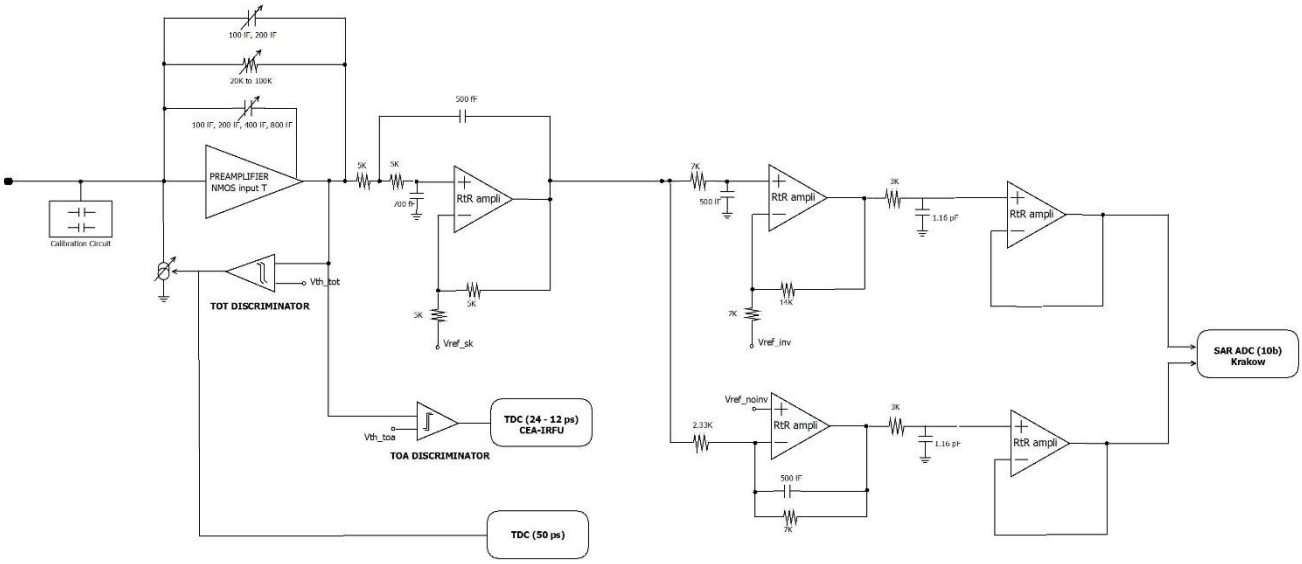
- The preamplifier part which converts the input charge coming from the SiPM to an output voltage. It must provide the first amplification of the signal with the best noise performance. The preamp stage is mad of a current conveyor with a variable gain and a charge variable charge preamp. The conveyor gives the ability to tune the preamp input voltage via a channel wise DAC.

  In the linear part of the amplifier, the feedback capacitors and feedback resistors provide the gain and the shape of the output signal which is send to the shaper. From the saturation and above, the feedback discriminator triggers and provides the charge measurement by using the “Time Over Threshold” technique (TOT). Another discriminator allows to give the timing information.

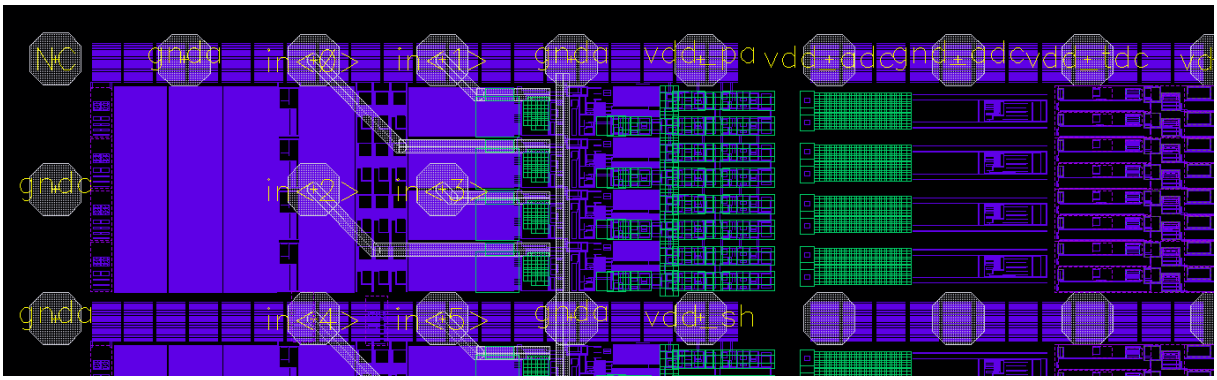
  The preamplifier can be calibrated by injecting a voltage step through two channel-wise selectable capacitors (0.5pF and 8pF).

- The shaper part is composed of three stages: a Sallen-Key filter, a RC² filter and a unity gain amplifier to drive the ADC. The shaping time can be adjusted over +/- 20% to compensate for process variations and ensure out of time pileup below 20%.

- The two discriminators providing the TOT and TOA (Time of Arrival) pulses, each one sent to a dedicated TDC.



In order to accommodate the C4 bump bonding pattern, the layout was entirely redone in order to fit in 120 µm height and avoid sensitive analog electronics below the bumps. Four channels fit between two rows of pads and the slow control, common to 4 channels, is placed below the pads.



In addition to the 72 readout channels, there are 4 channels for common mode subtraction and 2 channels for MIP calibration. The common mode channels are similar to the regular channels except they stop at the ADC (there are not TDCs). They do not enter the trigger path but are read out in the data path.

In the following sections, more details are given for each blocks.

1.1.1 Preamplifier

The preamplifier is DC coupled to the input and provides three outputs:

- Out_pa connected to the **shaper** and the **TOT discriminator**. Its DC operating point is the same than the preamplifier input (160 - 200 mV).

- Out_pa_time connected by default to the **TOA discriminator**. Its DC operating point is around outpa + Vgs (~ 500 mV).

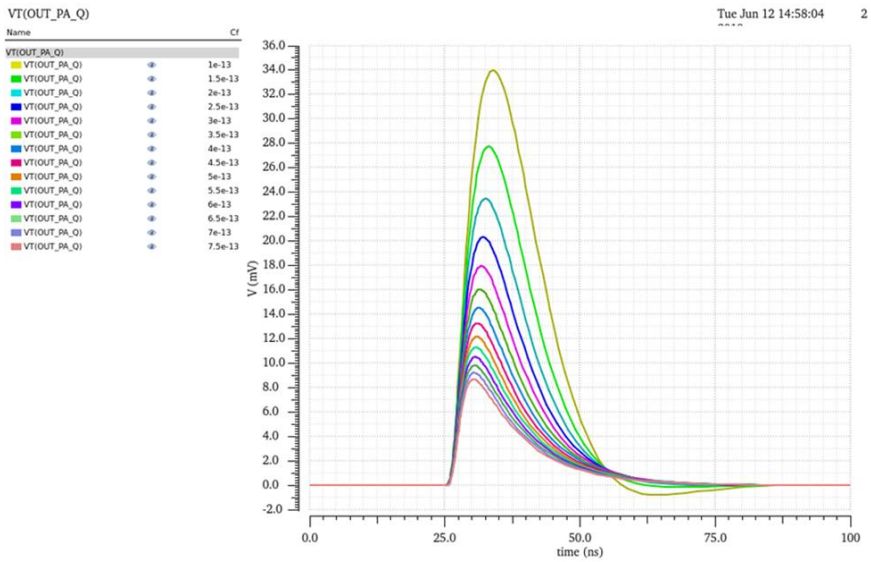
A 6b-DAC is connected channel wise to the preamplifier input to tune the DC level at the input and adjust the SiPM bias voltage.

A current 6b-DAC is connected channel wise also to compensate the current in the preamp feedback resistor.

The purpose of the preamplifier is to convert the input charge to a voltage output with the best signal-to-noise ratio and a gain adapted to the MIP signal. It must also provide a "short" signal duration to mitigate the Out-of-Time pileup effect at the shaper output. To meet all these requirements, the gain and the time constant must be adjustable **(these parameters are global, not channel-wise)**. In the table below, all the possibility are described:

Cd (pF)	5pF;10pF;20pF	A the conveyor output and at the preamp input. To ensure the preamp stability
Rf (Ω)	10k,15k,20k,25k	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get a decay time constant around 10 ns.
Cf (fF)	50,100,200,40fF	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50,100,200,400fF	Same purpose than Cf capacitors, but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

The following plot shows the preamplifier response to a 10 fC input charge for different choice of gain. The feedback resistor is adjusted so that the Rf*Cf product is constant and so the "duration" of the signal. As can be seen in Fig. , an undershoot appears for the highest preamp gain.



In the table below, all the parameters concerning the preamplifier are described.

Preamplifier parameters

Name	# bits	I2C Sub-block / sub-address	Description
Dacb<5:0>	1	Channel-wise	Current dac for preamp DC current compensation
Sign_Dacb	1	Channel-wise	Sign for Current dac for preamp DC current compensation
Inputdacb<5:0>	6	Channel-wise	Input dac for SiPM Biasing adjustement
Probe_pa	1	Channel-wise	Preamplifier output probe
LowRange	1	Channel-wise	0.5pF injection cap
HighRange	1	Channel-wise	8pF injection cap
Channel_off	1	Channel-wise	"1" = preamplifier input tied to ground
Vb_conv<5:0>	6	Global-analog	conveyor current bias
Vbi_pa<5:0>	6	Global-analog	Preamp current bias
ON_pa	1	Global-analog	"1" = enable preamplifier bias
ON_time	1	Global-analog	"1" = enable preamp fast output bias
Sw_super_conv	1	Global-analog	"1" = enable "super conveyor"
Conv_gain	4	Global-analog	Conveyor Gain: **<0> = 0.025, <1> = 0.05, <2> = 0.1, <3> = 0.2**
Cd<2:0>	3	Global-analog	Input preamp cap**. <0> = 5pF, <1> = 10pF, <2> = 20pF,** In //
Cf<3:0>	4	Global-analog	Preamp feedback cap**. <0> = 50fF, <1> = 100fF, <2> = 200fF, <3> = 400fF** In //
Cf_comp<3:0>	4	Global-analog	Preamp feedback comp. cap. : **<0>=50fF, <1> = 100fF, <2> = 200fF, <3>=400fF** In //
Rf<3:0>	4	Global-analog	Preamp feedback Res. **<3> = 25K, <2> = 20K, <1> = 15K, <0> = 5K** In //
Calib_dac<11:0>	12	Voltage references	Calibration DAC value
IntCtest	1	Voltage references	Selection of the Calibration DAC
ExtCtest	1	Voltage references	Selection of the external pulse test

Since the preamplifier converts an input charge to an output voltage, its behaviour over the entire charge dynamic must be well known and characterized. That can be divided in three steps:

- The linear mode: the preamplifier provides an output amplitude proportional to the input charge. It is able to provide linear amplitude over ~300mV dynamic range[1] (see red curves in the following plot). The ADC is used to measure the charge in this region which is named ADC range.
- The non-linear mode: this mode occurs in-between the linear and the saturated modes when the preamplifier is no longer linear but not still fully saturated. It is in this region that the TOT threshold has to be set in order to optimize the ADC range linearity. The preamplifier non-

linear mode leads to the non-linearity of the TOT low range, but the pile-up limitation is expected to be the best in this region (see violet and blue curves in the following plot and red curves in the next). The non-linear mode occurs for an output amplitude between 500 and 600mV.

- The saturated mode: it occurs for an output amplitude above 600mV. In this region, the preamplifier pulse width is proportional to the input charge and so well suited to use the Time-over-Threshold technics. The drawback is the undershoot of the preamplifier signal leading to incorrect charge measurement in the next bunch crossing. The undershoot is due to the fact that in saturation the preamplifier is in open loop and consequently slower to recover its normal behaviour.

1.1.2 Shapers

The shaper is divided in three stages:

- A Sallen-Key (S-K) shaper
- An Amplifier
- Then a buffer to drive the ADC

Two global 10b-DACs allow the user to adjust the DC levels, and so the pedestal of the shaper outputs. One additional local 5b-DAC allows to reduce the dispersion of the pedestals per channel.

Shaper parameters

Name	# bits	I2C Sub-block / sub-address	Description
Probe_noinv	1	Channel-wise	Non inverter shaper output probe (“1” = selected)
Probe_inv	1	Channel-wise	Inverter shaper output probe (“1” = selected)
Ref_dac_inv<4:0>	5	Channel-wise	Local 5b-DAC for ADC pedestal tuning
ON_rtr	1	Global-analog	“1” = enable shaper amplifiers bias
Ibi_sk<1:0>	2	Global-analog	S-K amplifier input stage current
Ibo_sk<5:0>	6	Global-analog	S-K amplifier output stage current
S_sk<2:0>	3	Global-analog	S-K amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_inv<1:0>	2	Global-analog	Inverter amplifier input stage current
Ibo_inv<5:0>	6	Global-analog	Inverter amplifier output stage current
S_inv<2:0>	3	Global-analog	Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_noinv<1:0>	2	Global-analog	Non Inverter amplifier input stage current
Ibo_noinv<5:0>	6	Global-analog	Non Inverter amplifier output stage current
S_noinv<2:0>	3	Global-analog	Non Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_inv_buf<1:0>	2	Global-analog	Inverter buffer input stage current
Ibo_inv_buf<5:0>	6	Global-analog	Inverter buffer output stage current
S_inv_buf<2:0>	3	Global-analog	Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
Ibi_noinv_buf<1:0>	2	Global-analog	Non Inverter buffer input stage current

Ibo_noinv_buf<5:0>	6	Global-analog	Non Inverter buffer output stage current
S_noinv_buf<2:0>	3	Global-analog	Non Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
Inv_vref<9:0>	10	Voltage references	Inverter shaper global reference
Noinv_vref<9:0>	10	Voltage references	Non Inverter shaper global reference

1.1.3 Discriminators

There are two discriminators per channel, one for the TOT measurement, the other for the TOA.

The TOT discriminator is connected on the "out_pa output" of the preamplifier (160 – 200 mV). The TOA discriminator is connected to the "out_pa_time" output of the preamplifier (~ 500 mV). Two global 10b-DACs allow the user to adjust the thresholds of the discriminators and two local 5b-DACs allow to reduce the dispersion per channel.

There are two external trigger inputs available; typically, in the case when the user wants to calibrate the TOT and TOA, he can send a trigger for the TOA discriminator and the other for the TOT discriminator. He can also send a trigger for a channel, and the other for a neighbouring channel.

The two discriminators outputs can be masked per channel as well.

Regarding the TOT discriminator, when it is triggered (output at 0), it enables a constant current source which discharges the preamplifier so that the duration of the preamp signal is proportional to the input charge. This current source can be adjusted over 6 bits in order to adjust the width of the TOT (nominal specification is 200ns for 10 pC).

The two discriminators outputs can be probed and looked at on a scope.

Discriminators parameters

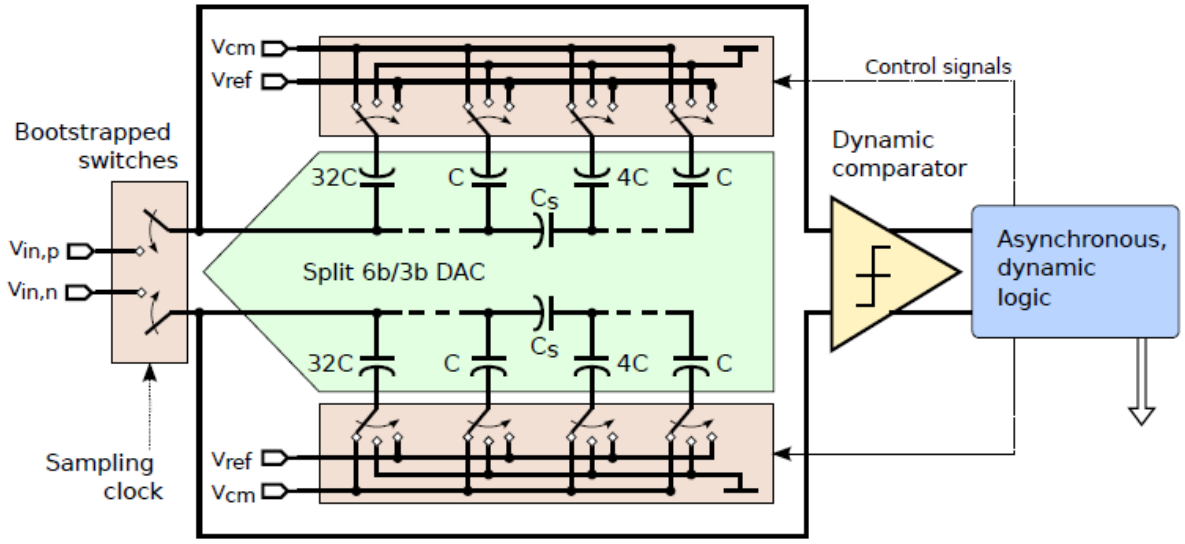
Name	# bits	I2C Sub-block / sub-address	Description
Ref_dac_toa<4:0>	5	Channel-wise	Local 5b-DAC for TOA threshold tuning
Ref_dac_tot<4:0>	5	Channel-wise	Local 5b-DAC for TOT threshold tuning
Mask_toa	1	Channel-wise	TOA discri output mask ("1" = masked)
Sel_trigger_toa	1	Channel-wise	External trigger selection for TOA ("0" = Ext Trig1; "1" = Ext Trig2)
Sel_trigger_tot	1	Channel-wise	External trigger selection for TOT ("0" = Ext Trig1; "1" = Ext Trig2)
Mask_tot	1	Channel-wise	TOT discri output mask ("1" = masked)
Probe_tot	1	Channel-wise	TOT discri output probe
Probe_toa	1	Channel-wise	TOA discri output probe
ON_toa	1	Global-analog	"1" = enable TOA discri bias
ON_tot	1	Global-analog	"1" = enable TOT discri bias
Dac_itot<5:0>	6	Global-analog	6b-DAC for TOT gain tuning ("000000" = no feedback current as the original TOT architecture)
Sel_input_toa	1	Global-analog	"0" = charge output; "1" = fast output
En_hyst_tot	1	Global-analog	"1" = enable the TOT discri hysteresis

Pol_trig_toa	1	Global-analog	Polarity of the TOA discri output
Tot_vref<9:0>	10	Voltage references	TOT threshold global value
Toa_vref<9:0>	10	Voltage references	TOA threshold global value

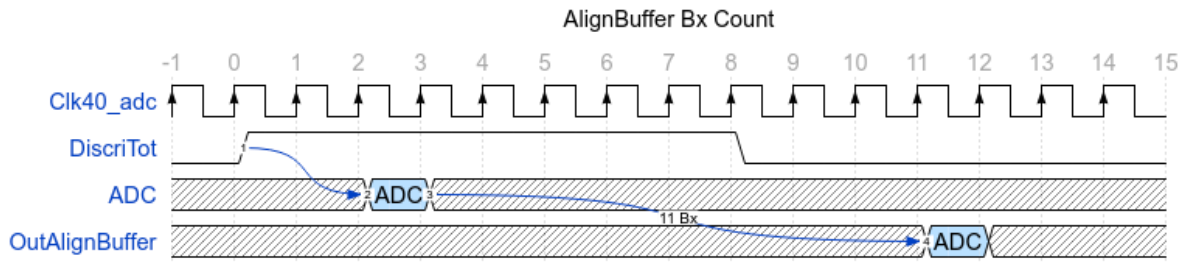
1.2 Mixed-signal blocks

1.2.1 10 bits ADC and Align Buffer

Both chips, HGCROC2 and HGCROC2A, embed two versions of ADC, designed by AGH in Krakow. For channels 36 to 71, there is a silicon-proven ADC with vrefm reference voltage tied to ground. For channels 0 to 35, a new version of the ADC was submitted with a dedicated vrefm set at 100 mV (nominal).



The 10 bits data provided by the ADC are sent to an Align Buffer to align them to the TOT and TOA data. Indeed, the TDCs providing the TOT measurement introduce a latency due to the duration of the TOT itself (this latency is tuneable in the TDCs). The ADC + Align Buffer have a fixed latency of 11 bunch crossings: sampling at BC=1, ADC data available at BC=2, data at the Align Buffer ouputs at BC=11 (see next chronogram).



ADC parameters

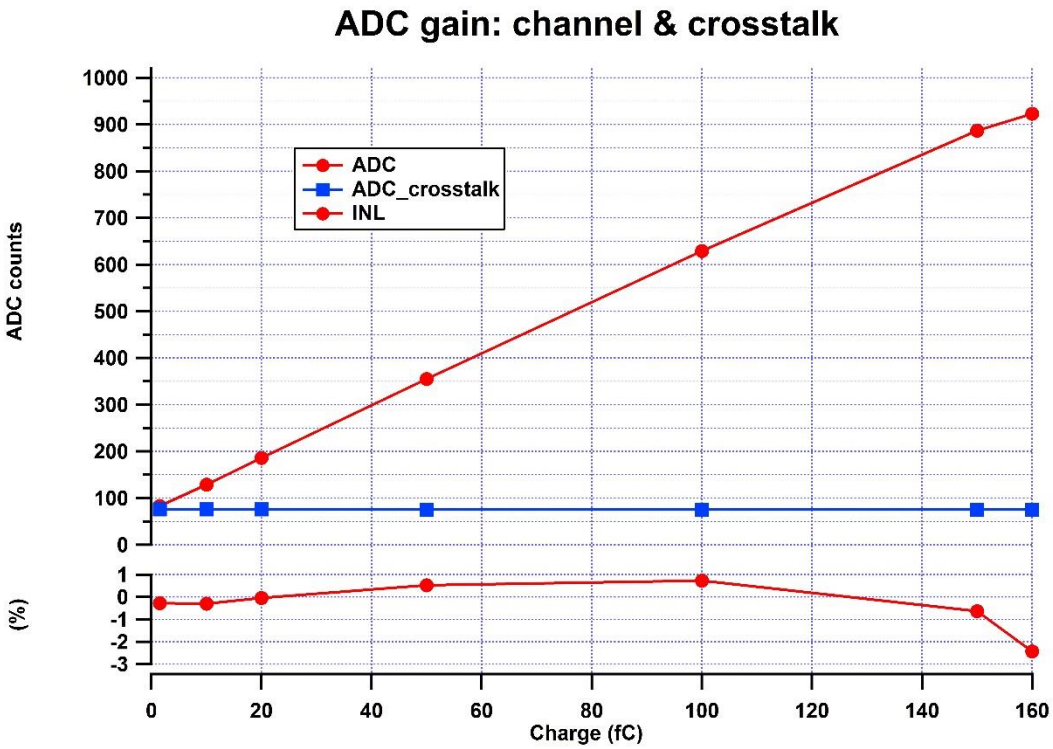
Name	# bits	I2C Sub-block / sub-address	Description
Mask_adc	1	Channel-wise	“1” = ADC clock off
maskAlignBuffer	1	Channel-wise	“1” = AlignBuffer clock off
Adc_pedestal<7:0>	8	Channel-wise	ADC pedestal value
ExtData<9:0>	10	Channel-wise	Forced ADC data
Clr_ShaperTail	1	Global-analog	
SelRisingEdge	1	Global-analog	“1” = AlignBuffer provides data on rising edge
SelExtADC	1	Global-analog	“1” = Forced ADC data send to the DRAM
Clr_ADC	1	Global-analog	
Ref_adc<1:0>	2	Global-analog	Input stage current of the Ref ADC OTA
Delay40<2:0>	3	Global-analog	Delay tuning for bits <4:0> “000” = faster conversion
Delay65<2:0>	3	Global-analog	Delay tuning for bits <6:5> “000” = faster conversion
Delay87<2:0>	3	Global-analog	Delay tuning for bits <8:7> “000” = faster conversion
Delay9<2:0>	3	Global-analog	Delay tuning for bit <9> “000” = faster conversion
ON_ref_adc	1	Global-analog	“1” = enable ADC ref OTA
Pol_adc	1	Global-analog	ADC input swap

The Align Buffer also performs the pedestal subtraction.

The user can choose to force ADC data to 0 when the TOT pulse is at 1 (Clr_ADC=”1”), otherwise it provides the actual ADC values.

As after a TOT the shaper returns to the pedestal after a given time, the user can also choose to force ADC data to 0 for two next bunch crossing after the end of the TOT pulse (Clr_ShaperTail=”1”).

The following plot shows the linearity and the INL expressed in % of the ADC range in the default parameters setting.



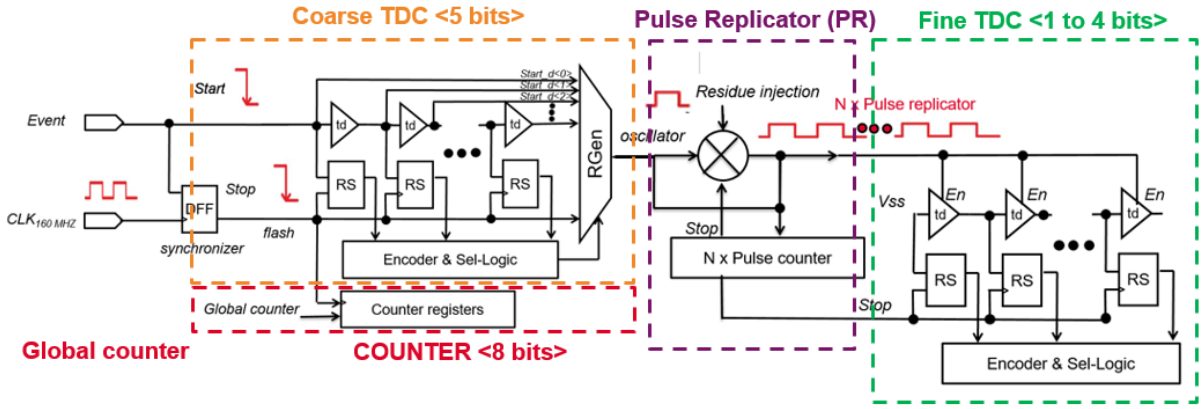
1.2.2 TOT and TOA TDCs

One TDC block handles the TOA and TOT measurements. It was designed by the CEA IRFU group in Saclay. The two following tables give the specifications respectively for the TOA and the TOT.

TDC ToA specifications	
Resolution	about 25 ps RMS
Range	10 bits over 25 ns
Conversion rate	> 40 MHz (bunch clock)
Power consumption	< 2 mW / channel
Area	Pitch 120 µm
Technology	TSMC 130 nm
Temperature	-30 °C

TDC ToT specifications	
Resolution	< 50 ps RMS
Range	12 bits over 2-200 ns
Min time between hits	25 ns
Power consumption	< 2 mW / channel
Fixed latency	12 clock periods
Technology	TSMC 130 nm
Area	Pitch 120 µm
Temperature	-30 °C

The schematic below gives an overview of the TDC circuitry.



More detailed explanations about circuit, functionality and configuration can be found in dedicated documentation:

- **HGCROC_TOA_TOT_PLL_SPECIFICATIONS.pdf** describing the specifications of all parts designed by IRFU
- **SC_TDC_PLL_blocs.docx** where the user will find descriptions, default values of all slow control parameters of the two TDCs and the PLL
- **PLL and multi-channel TDC for HGCROCv2 TestPhase preparation.pdf** where is described the tests to be performed for characterizing the PLL and the TDCs;

TDCs parameters

Name	# bits	I2C Sub-block / sub-address	Description
DIS_TDC	1	Channel-wise	Disable TDC channel (enable by default)
DAC_CAL_CTDC_TOA <0:5>	6	Channel-wise	Tune the fine gain of the TOA CTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
DAC_CAL_FTDC_TOA <0:5>	6	Channel-wise	Tune the fine gain of the TOA FTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
DAC_CAL_CTDC_TOT <0:5>	6	Channel-wise	Tune the fine gain of the TOT CTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
DAC_CAL_FTDC_TOT <0:5>	6	Channel-wise	Tune the fine gain of the TOA FTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
IN_FTDC_ENCODER_TOA<0:5>	6	Channel-wise	Adjust the ToA FTDC offset by 5 bits <0:4> and the sign 1 bit <5>

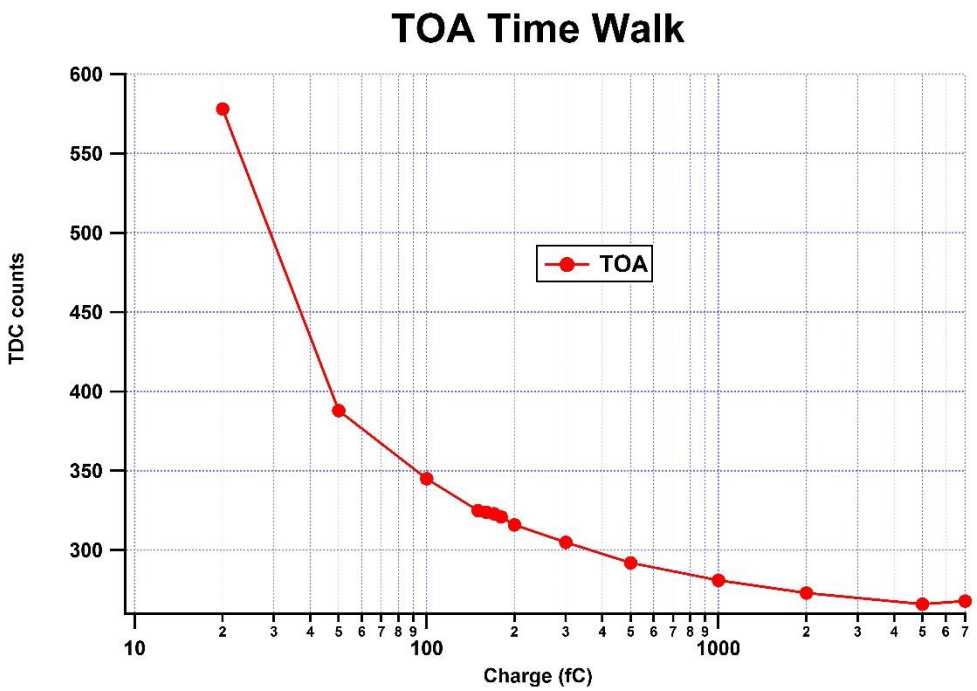
			OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
IN_FTDC_ENCODER_TOT<0:5>	6	Channel-wise	Adjust the ToT FTDC offset by 5 bits <0:4> and the sign 1 bit <5> OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
GLOBAL_TA_SELECT_GAIN_TOT<0:3>	4	Master TDC	ToT pulse replicator gain : '1000' : 2 pulses (TDC LSB : 97,6 ps) **'1100' : 4 pulses (TDC LSB : 48,8 ps) (Default)** '1110' : 8 pulses (TDC LSB : 24,4 ps) '1111' : 16 pulses (TDC LSB : 12,2 ps)
GLOBAL_TA_SELECT_GAIN_TOA<0:3>	4	Master TDC	ToA pulse replicator gain : '1000' : 2 pulses (TDC LSB : 97,6 ps) '1100' : 4 pulses (TDC LSB : 48,8 ps) **'1110' : 8 pulses (TDC LSB : 24,4 ps) (Default)** '1111' : 16 pulses (TDC LSB : 12,2 ps)
GLOBAL_SEU_TIME_OUT	1	Master TDC	Activate the SEU time-out in the control logic channel
GLOBAL_MODE_FTDC_TOA_S0 & S1 <S0:S1>	2	Master TDC	ToA pulse replicator gain : S0 & S1 for the digital substation ToT – ToA <S0:S1> '00' : 2 pulses (TDC LSB : 97,6 ps) '10' : 4 pulses (TDC LSB : 48,8 ps) **'01' : 8 pulses (TDC LSB : 24,4 ps) (Default)** '11' : 16 pulses (TDC LSB : 12,2 ps)
GLOBAL_LATENCY_TIME<0:3>	4	Master TDC	Configure the latency time windows for data output synchronization with 40 MHz CLK '0000': direct 0 s **'0101': 10 CLK latency** '1111': 15 CLK latency
GLOBAL_MODE_NO_TOT_SUB	1	Master TDC	Disable the digital substation ToT – ToA ToT output = ToT without substation
GLOBAL_MODE_TOA_DIRECT_OUTPUT	1	Master TDC	The output of the ToA TDC are directly connected to the ToA & ToT output
GLOBAL_DISABLE_TOT_LIMIT	1	Master TDC	Disable ToT auto limit max to '1' for the ToT test
GLOBAL_FORCE_EN_TOT	1	Master TDC	Force the ToT flag event to '1' (always read ToT)
GLOBAL_FORCE_EN_OUTPUT_DATA	1	Master TDC	Force the En flag event to '1' (always read ToA)
GLOBAL_FORCE_EN_CLK	1	Master TDC	Force the output data transfer clk (always clock gating) '0' : 2 clk cycles dedicated to 1 data transfer (1 for the data & 1 for the 0 after) (low power mode) '1' : clk is always present for the data transfer (40 MHz power consumption)
EN_REF_BG	1	Master TDC	Activate the BANDGAP source 1V to the calibration part '0' : External PAD 'EXT_REF_TDC' **'1' : Internal 1V Bandgap 'BG_1V'**
CALIB_CHANNEL_DLL	1	Master TDC	Activate the automatic calibration of all TDC channel
START_COUNTER	1	Master TDC	Activate the global gray counter for the TDC channel (rising edge for the 40 MHz 160 MHz synchronization)
INV_FRONT_40MHZ	1	Master TDC	Inverse the 40 MHz front for the gray counter and the SEU_TIME_OUT
BIAS_FOLLOWER_CAL_P_EN	1	Master TDC	Enable the VTC follower for the channel TDC calibration follower bias P
BIAS_FOLLOWER_CAL_P_D<0:3>	4	Master TDC	Configure the VTC follower for the channel TDC calibration follower bias P current : Current = DATA<0:3> Weight addition **'base' : 50 nA** <0>: 100 nA <1>: 500 nA <2>: 2,5 µA <3>: 5 µA
EN_MASTER_CTDC_DLL	1	Master TDC	Activate the CTDC master DLL to provide master CLKs and global channel calibration : '0' : OFF : No CLKs "power off channels" **'1' : ON : MASTER TDC activated (Default)**
EN_MASTER_CTDC_VOUT_INIT	1	Master TDC	Activate the voltage load in "VD_CTDC_P" of the master CTDC DLL pump charge output : **'0' : High Z pump charge (Default)**

			'1' : CTDC_P INIT voltage load « VD_CTDC_P_DAC MODE»
VD_CTDC_P_DAC_EN	1	Master TDC	Activate the DAC for the VD_CTDC_P voltage : '0' : external PAD "VD_CTDC_P_EXT" '1' : 5 bits DAC "VD_CTDC_P_D<0:4>"
VD_CTDC_P_D<0:4>	5	Master TDC	5 bits DAC for the VD_CTDC_P voltage : '00000' = 0,2 V '11111' = 0,75 V
CTDC_CALIB_FREQENCY<0:5>	6	Master TDC	CTDC Master DLL calibration period : '000000' : 32 ns '100000' : 50 ns **'010000' : 100 ns** '001000' : 200 ns '000100' : 400 ns '000010' : 800 ns '000001' : 1600 ns '111111' : 3200 ns
FOLLOWER_CTDC_EN	1	Master TDC	Activate the VTC for the bias MASTER CTDC BIAS_N_CTDC bias (pump charge injection): '0' : OFF **'1' : VTC 6 bits "BIAS_I_CTDC_D<0:5>**
BIAS_I_CTDC_D<0:5>	6	Master TDC	Configure the VTC the bias CTDC BIAS_N_CTDC bias (pump charge injection current) : Current = DATA<0:5> Weight addition (**default 30 µA**) 'base' : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 µA <3>: 5 µA <4>: 25 µA <5>: 50 µA
VD_CTDC_N_DAC_EN	1	Master TDC	Activate the DAC for the VD_CTDC_N voltage : '0' : external PAD "VD_CTDC_N_EXT" '1' : 5 bits DAC "VD_CTDC_N_D<0:4>"
VD_CTDC_N_D<0:4>	5	Master TDC	5 bits DAC for the VD_CTDC_N voltage : '00000' = 0,6 V '11111' = 1 V
VD_CTDC_N_FORCE_MAX	1	Master TDC	**Force the VD_CTDC_N voltage to 1,2 V**
GLOBAL_EN_BUFFER_CTDC	1	Master TDC	Enable the BUFFER of the calibration CTDC channel **'0' : OFF** '1' : 'VTC 6 bits "BIAS_CAL_DAC_CTDC_P_D<0:3>'
BIAS_CAL_DAC_CTDC_P_EN	1	Master TDC	Activate the VTC for the bias BIAS_CAL_DAC_CTDC_P bias of the current calibration channel **'0' : OFF** '1' : VTC 6 bits 'BIAS_CAL_DAC_CTDC_P_D<0:3>'
BIAS_CAL_DAC_CTDC_P_D<0:3>	4	Master TDC	Configure the VTC BIAS_CAL_DAC_CTDC_P bias of the current calibration channel: Current = DATA<0:5> Weight addition <0>: 100 nA <1>: 500 nA <2>: 1 µA <3>: 4 µA
GLOBAL_INIT_DAC_B_CTDC	1	Master TDC	Load the channel calibration registers by DAC_CAL_CTDC_TOA <0:5> and DAC_CAL_CTDC_TOT <0:5> **'0' : LOAD by SC registers** '1' : Adjustment in automatic calibration mode
CTRL_IN_SIG_CTDC_P_EN	1	Master TDC	Activate the DAC for CTRL_SIG_CTDC calibration voltage : **'0' : DAC OFF 0 V output** '1' : DAC 5 bits "CTRL_IN_SIG_CTDC_P_D<0:4>"
CTRL_IN_SIG_CTDC_P_D<0:4>	5	Master TDC	5 bits DAC for the CTRL_SIG_CTDC calibration voltage : '00000' = 0,2 V '11111' = 0,8 V
CTRL_IN_REF_CTDC_P_EN	1	Master TDC	Activate the DAC for CTRL_REF_CTDC calibration voltage :

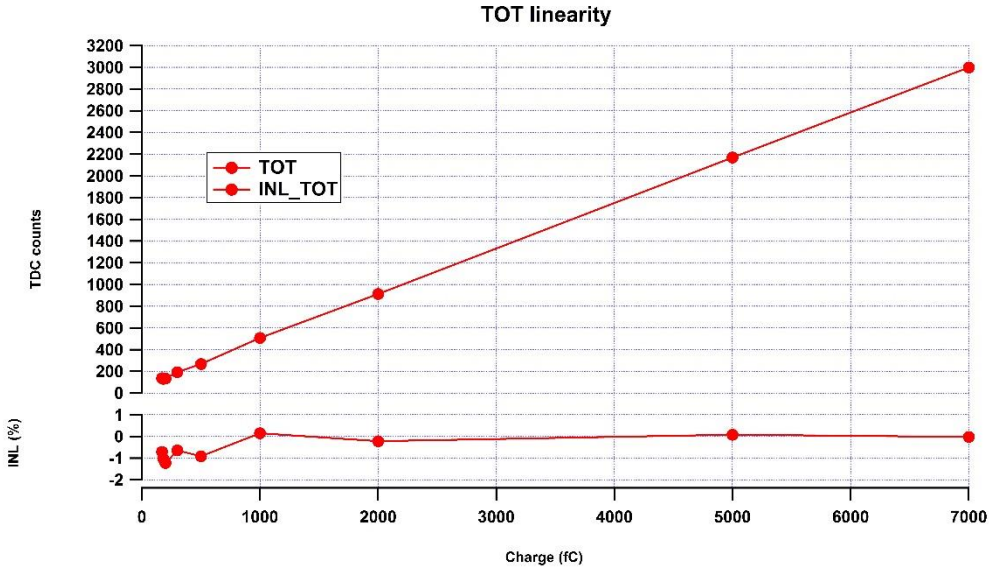
			'0' : DAC OFF 0 V output '1' : 5 bits DAC "CTRL_IN_REF_CTDC_P_D<0:4>"
CTRL_IN_REF_CTDC_P_D<0:4>	5	Master TDC	DAC 5 bits for the CTRL_REF_CTDC calibration voltage : '00000' = 0,2 V '11111' = 0,8 V
EN_MASTER_FTDC_DLL	1	Master TDC	Activate the FTDC master DLL to provide master CLKs and global channel calibration : '0' : OFF : No CLKs "power off channels" **'1' : ON : MASTER TDC activated (Default)**
EN_MASTER_FTDC_VOUT_INIT	1	Master TDC	Activate the voltage load in "VD_FTDC_P" of the master FTDC DLL pump charge output : **'0' : High Z pump charge (Default)** '1' : FTDC_P INIT voltage load « VD_FTDC_P_DAC MODE»
VD_FTDC_P_DAC_EN	1	Master TDC	Activate the DAC for the VD_FTDC_P voltage : '0' : external PAD "VD_FTDC_P_EXT" '1' : 5 bits DAC "VD_FTDC_P_D<0:4>"
VD_FTDC_P_D<0:4>	5	Master TDC	5 bits DAC for the VD_FTDC_P voltage : '00000' = 0,4 V '11111' = 0,9 V
FTDC_CALIB_FREQENCY<0:5>	6	Master TDC	FTDC Master DLL calibration period : '000000' : 32 ns '100000' : 50 ns **'010000' : 100 ns** '001000' : 200 ns '000100' : 400 ns '000010' : 800 ns '000001' : 1600 ns '111111' : 3200 ns
FOLLOWER_FTDC_EN	1	Master TDC	Activate the VTC for the bias MASTER FTDC BIAS_N_FTDC bias (pump charge injection): '0' : OFF **'1' : VTC 6 bits "BIAS_I_FTDC_D<0:5>**
BIAS_I_FTDC_D<0:5>	6	Master TDC	Configure the VTC the bias FTDC BIAS_N_FTDC bias (pump charge injection current) : Current = DATA<0:5> Weight addition (**default 30 µA**) 'base' : 50 nA <0>: 100 nA <1>: 500 nA <2>: 2,5 µA <3>: 5 µA <4>: 25 µA <5>: 50 µA
VD_FTDC_N_DAC_EN	1	Master TDC	Activate the DAC for the VD_FTDC_N voltage : '0' : external PAD "VD_FTDC_N_EXT" '1' : 5 bits DAC "VD_FTDC_N_D<0:4>"
VD_FTDC_N_D<0:4>	5	Master TDC	5 bits DAC for the VD_FTDC_N voltage : '00000' = 0,4 V '11111' = 0,9 V
VD_FTDC_N_FORCE_MAX	1	Master TDC	**Force the VD_FTDC_N voltage to 1,2 V**
GLOBAL_EN_BUFFER_FTDC	1	Master TDC	Enable the BUFFER of the calibration FTDC channel **'0' : OFF** '1' : 'VTC 6 bits "BIAS_CAL_DAC_FTDC_P_D<0:3>'
BIAS_CAL_DAC_FTDC_P_EN	1	Master TDC	Activate the VTC for the bias BIAS_CAL_DAC_FTDC_P bias of the current calibration channel **'0' : OFF** '1' : VTC 6 bits 'BIAS_CAL_DAC_FTDC_P_D<0:3>'
BIAS_CAL_DAC_FTDC_P_D<0:3>	4	Master TDC	Configure the VTC BIAS_CAL_DAC_FTDC_P bias of the current calibration channel: Current = DATA<0:5> Weight addition <0>: 100 nA <1>: 500 nA <2>: 1 µA <3>: 4 µA

GLOBAL_INIT_DAC_B_FTDC	1	Master TDC	Load the channel calibration registers by DAC_CAL_FTDC_TOA <0:5> and DAC_CAL_FTDC_TOT <0:5> **'0' : LOAD by SC registers** '1' : Adjustment in automatic calibration mode
CTRL_IN_SIG_FTDC_P_EN	1	Master TDC	Activate the DAC for CTRL_SIG_FTDC calibration voltage : **'0' : DAC OFF 0 V output** '1' : DAC 5 bits "CTRL_IN_SIG_FTDC_P_D<0:4>"
CTRL_IN_SIG_FTDC_P_D<0:4>	5	Master TDC	5 bits DAC for the CTRL_SIG_FTDC calibration voltage : '00000' = 0,2 V '11111' = 0,8 V
CTRL_IN_REF_FTDC_P_EN	1	Master TDC	Activate the DAC for CTRL_REF_FTDC calibration voltage : **'0' : DAC OFF 0 V output** '1' : 5 bits DAC "CTRL_IN_REF_FTDC_P_D<0:4>"
CTRL_IN_REF_FTDC_P_D<0:4>	5	Master TDC	DAC 5 bits for the CTRL_REF_FTDC calibration voltage : '00000' = 0,2 V '11111' = 0,8 V

The following plot shows the digitized TOA time walk.



The following plot shows the TOT linearity and the INL expressed in % of the dynamic range.



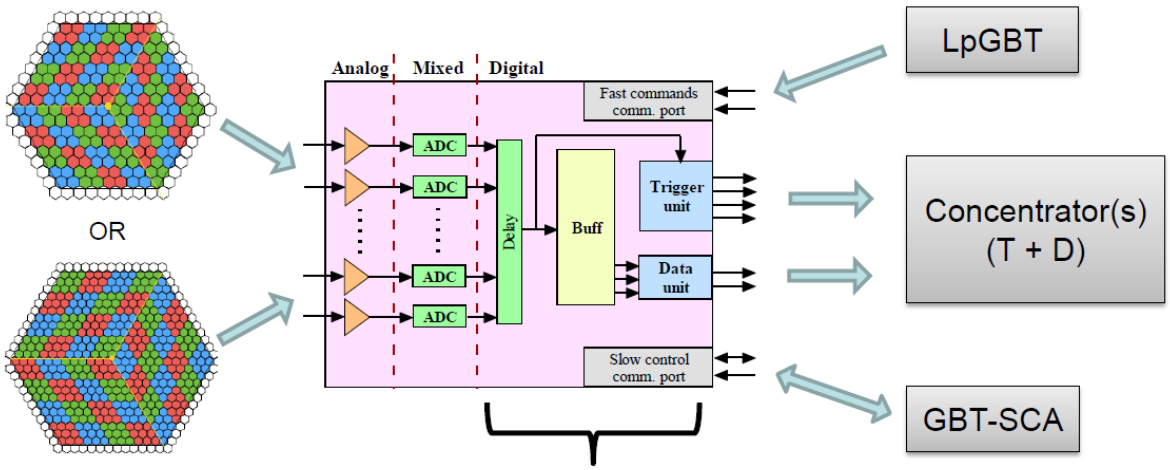
1.3 Digital blocks

The main specifications of the digital part of the ASIC are described in the table below.

Analog channels:	1) 72 analog channels 2) 4 for common mode 3) 2 for calibration
Acquisition mode:	Continuous @ Bx rate (40 MHz)
L1-functionnality:	Partial ➔ no derandomizer
L1-Trigger rate:	< 1 MHz (corresponding to max)
Daq readout mode:	1) Triggered by L1A 2) Continuous in debug mode 3) With acquisition stopped (like V1)
Trigger data type:	7-bit sums (4 or 9 channels)
Daq data type:	32 bits / channels
Trigger output port:	4 x CLPS @ 1280 Mbps
Daq output port:	2 x CLPS @ 1280 Mbps

HGCROC2 integrates 72 channels to readout

- 192 channels sensor with a 64-ch configuration
- 432 channels sensor with a 72-ch configuration



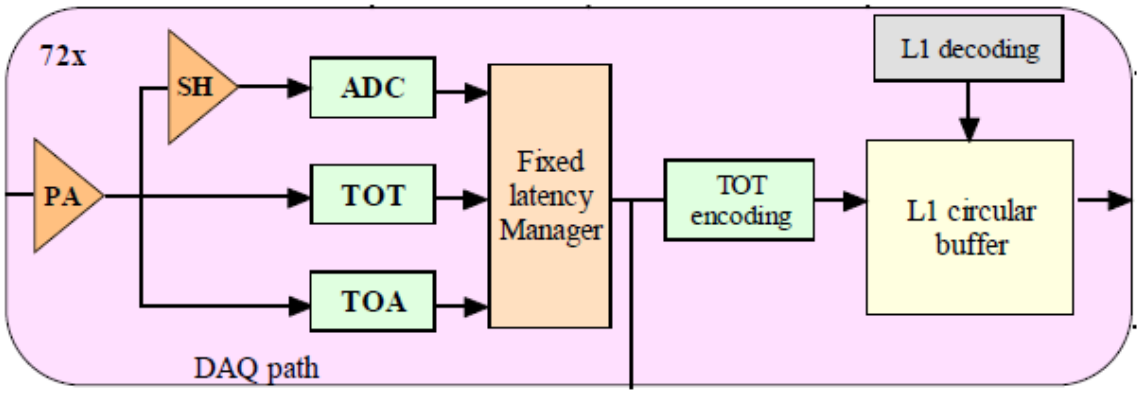
The document **HGROCv2_LinkSpecs_Guide.pdf** details the data path and the trigger path.

1.3.1 Data path

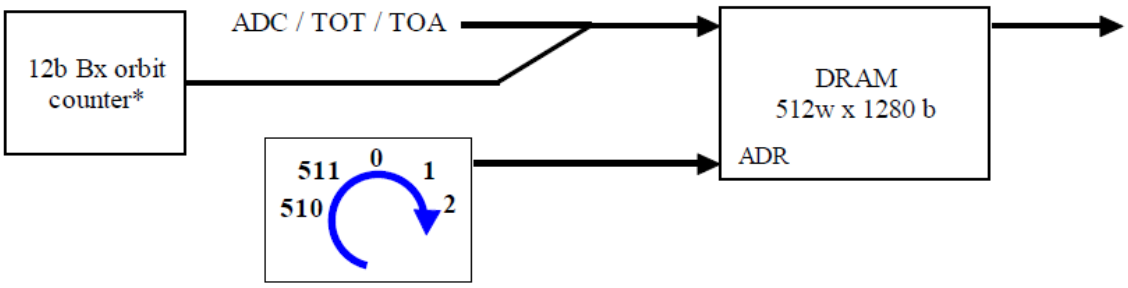
All the data coming from the ADC and the two TDCs are continuously memorized into a circular memory based on a DRAM architecture. The circular memory is 512 length and only L1-triggered data are read out. Two output differential port send out the data at 1.28 Gbps.

Special channels, common mode and calibration channels, provide only the ADC data.

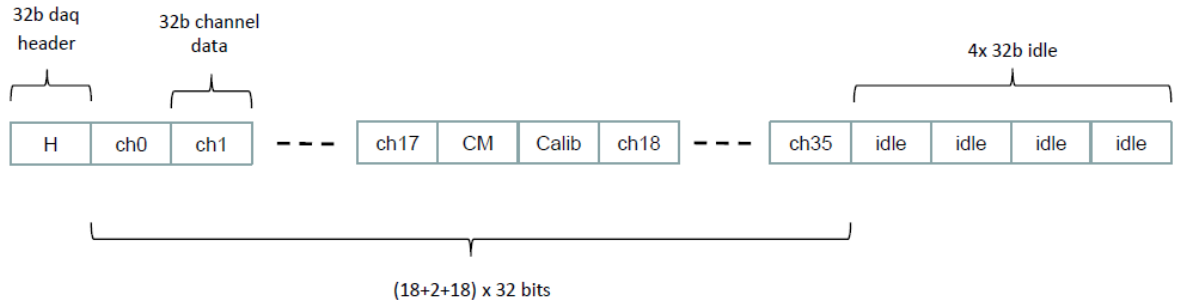
The figure below describes the functionality of the data path.



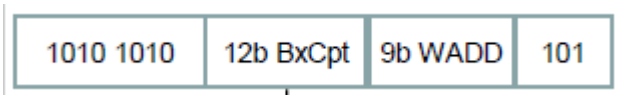
The ADC and the TOA data are over 10 bits each and the TOT in 12 bits. All these data are stored at 40 MHz continuously into the DRAM; there is the possibility to compress the TOT data to 10 bits. The DRAM memory is controlled as a circular memory. After receiving a L1 trigger, a readout of the selected BX data is activated (the offset of the L1 trigger is configurable by slow control).



An idle packet is continuously sent out when no L1 trigger is activated. This Idle packet is configurable by slow control. The data format is described in the figure below and is composed of 1376 bits.



The 32b header is as follow:



With BxCpt the number of the Bunch Crossing counter and WADD the column address of the L1-triggered event.

The 32b data of channels are described in the table below.

SelRawData	TOT b11 to b0	TOA	ADC		32-b channel data
0	0	L	M		10 | 10b «0..0 » | 10b « L » | 10b « M »
0	K b11,b10,b9 = 000	L	M		10 | 10b K [0,b8:b0] | 10b « L » | 10b « 1..1»
0	K Other cases	L	M		10 | 10b K [1,b11:b3] | 10b « L » | 10b « 1..1»
1	K	L	M		12b K | 10b « L » | 10b « M »

1.3.2 Trigger path

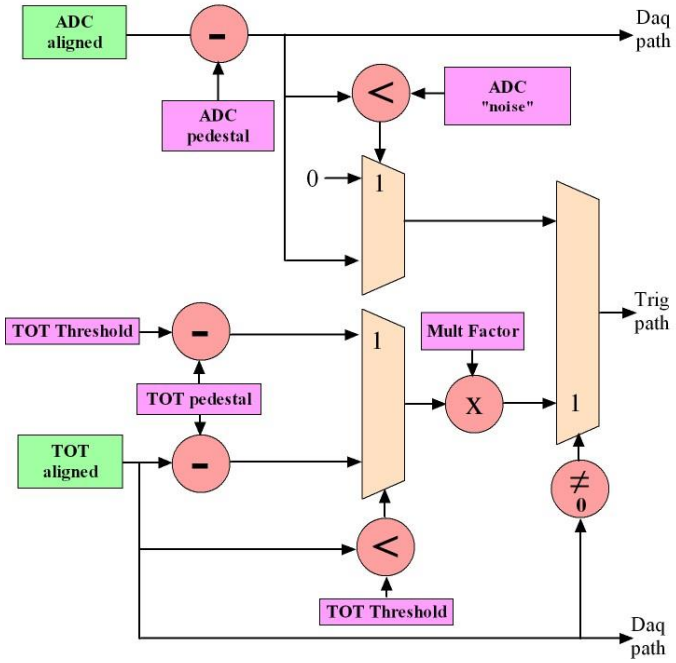
The data processing for the trigger path is composed as per below:

- Charge linearization over ADC/TOT range
- Sum of 4 or 9 channels depending on the sensor
- Charge compression to fit the bandwidth

The parameters involved in the charge linearization are:

- ADC pedestal to be subtracted

- TOT pedestal to be subtracted
- ADC threshold to force TOT to 0 if below
- TOT threshold to define the non-linear part of the TOT
- Multiplication factor with a LSB ratio between TOT and ADC

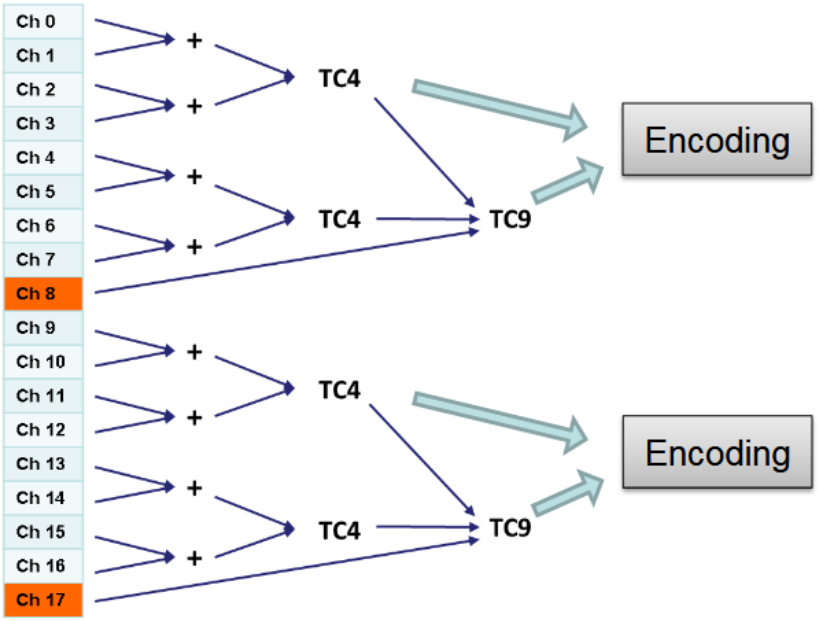


The value of the Multiplication factor allows to linearize the ADC range and the TOT range; it is coded over 5 bits in order to cope with the three typical gains:

- 31 for the 80fC ADC range
- 15.6 for the 160fC ADC range
- 7.8 for the 320fC ADC range

(The default slow control value is 25 for a theoretical 100fC ADC range.)

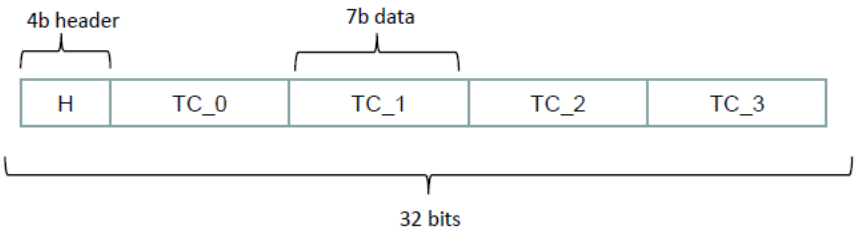
The schematic below describes the principle of the trigger sums for low density and high density sensors.



After the linearization, the selection between the sum by 4 (TC4) or 9 (TC9) is done by the ASIC parameter “SelTC4”.

The table below gives an overview of the trigger path output format.

# Trig-link	4 or 2
Link type / speed	CLPS @ 1280 Mbps
Possible to switch-off unused link	Yes
# bits in 1 packet (each 25ns)	32
Packet composition (see below)	During startup: 1 header + 28-bit idle word else: 1 header + 4x Trigger Cell sums
Header	4 bits « 1010 » or « 1001 » @ Bx0
Trigger Cell mapping	See next slide
Trigger cell (TC) encoding	4b Exponent + 3b Mantissa
Bits order	MSB first



1.3.3 Digital parameters

The table below gives all the parameters of the digital block for the data and trigger paths, thus there are two of them in the chip as there are two digital blocks for the both sides of the chip.

name	# bits	comment
PllLocked	1	If available, status of PLL locked
CmdSelEdge	1	0: select fall edge for fast commands sampling (default)
SelTC4	1	1: sum by 4 / 0: sum by 9
SelRawData	1	1: send raw digitized data into RAM
IdleFrame	28	Default 28 LSB "1100---1100" of idle DAQ/T frame
L1Offset	9	L1 offset corresponding to L1 latency
Adc_TH	4	Threshold corresponding to noise in ADC count
MultFactor	5	TOT vs ADC ratio for linearization (default ~25)
Tot_P0,Tot_P1,Tot_P2,Tot_P3	7	TOT pedestal used in TP (common to 9 channels)
Tot_TH0,Tot_TH1,Tot_TH2,Tot_TH3	8	TOT threshold used in TP (common to 9 channels)

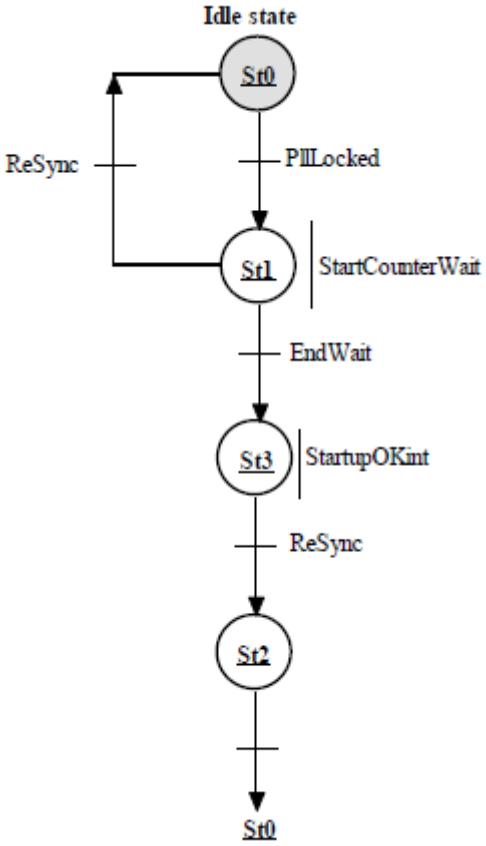
SelTCA, namely Select Trigger Cell of 4 channels, allows the user to select the sum mode: set to 1 to sum 4 channels, otherwise sum by 9.

SelTC4	# channels used	# ch in each TC	# Daq-link @ 1,28G	# Trig-link @ 1,28G	unused channels
0	72	9	2	2	-
1 (default)	64	4	2	4	(8, 17, 18, 27) (44, 53, 54, 63)

1.3.4 Startup Sequence

After each hard reset or "ReSync" commands, the startup sequence is initiated:

- It guarantees a minimum of 256 32b words of Idle packet for all serial links (Trigger and DAQ)
- 28 bits set by slow control (default 11 00 ---- 11 00) + 4b header set by bx0 (1010 else 1001)



The Daq link will complete current L1 transfer in case of ReSync command.

1.4 Interfaces blocks

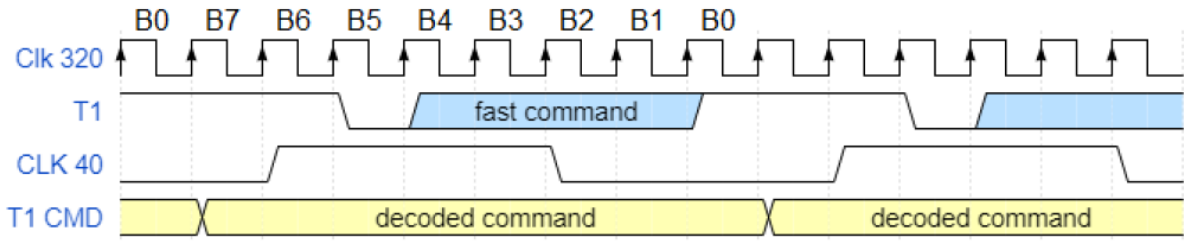
The document **HGCROCv2_configure_command_Guide.pdf** details the two following sections.

1.4.1 Fast command

All the ASICs receive, through LpGBT, a fast command link (data + clock):

- 1 link is composed by a clock at 320 MHz and a data “T1” link
- 8 bits command format: ‘110 xxxx 1’
- Synchronisation code: 110 (this code does not appear elsewhere in bitstream)
- Serial commands transmitted MSB first at 320 Mb/s

In HGCROC2/2A and H2GCROC2/2A, a minimum set of commands are decoded and used: Idle, CalibrationReq, L1A + clock synchronization (others are only decoded).



The available commands are described in the following table:

Fast command	B7 B0	description
IDLE	110 0000 1	Default command
Cmd_Orbit	110 0001 1	Reset internal Bx counter (seen in daq and trigger link header)
Cmd_Trigger	110 0100 1	Readout an event store in L1 buffer
Cmd_Calib	110 1000 1	Generate internal calibration pulse for the preamplifier
Cmd_Sync	110 1111 1	Force the startup mode (e-link synchronisation mode)
Cmd_Dump	110 1011 1	Internal use only (memory dump)

1.4.2 I2C

I2C protocol is used to access ASIC parameters. Main features are given in the table below:

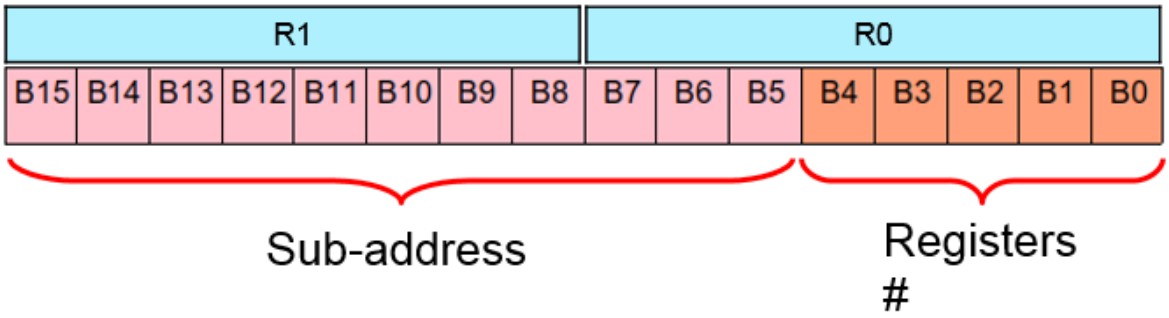
I2C	Detail	Comments
Chip addressing	4 bits	MSB of I2C first byte
Direct-access register addressing	3 bits	Register R0 to R7
"Burst" writing / reading	Yes	Accessible through R3
I2C speed	1M (max)	To be measured on HGCROCDv2
TMR	Yes	

The I2C circuits of the chip has 8 internal registers whose the use is described in the table below:

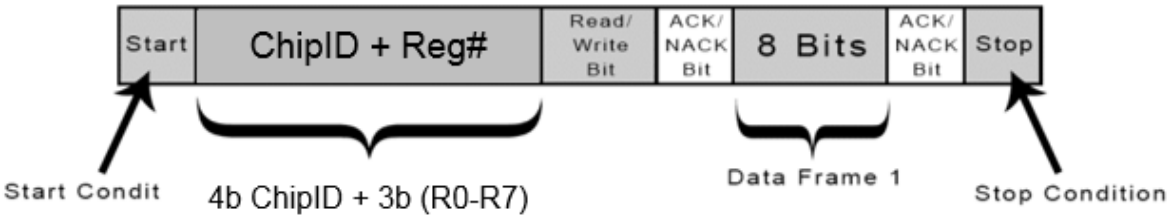
I2C @	Register	Comments
R0	ASIC parameter address (LSB)	Indirect @
R1	ASIC parameter address (MSB)	Indirect @
R2	Data	
R3	Data with auto @++	Increment indirect @ after each access
R4-R5-R6	Direct access SC-register	
R7	Status register (error, parity)	Read-only

To cope with the large number of parameters, extended addressing is used:

- 512 sub_address can be addressed (B15, B14 not used and have to be set to 0)
- Each sub_address has max 32 configuration parameters
- Extended addressing realized through 2 direct access registers: R0 and R1

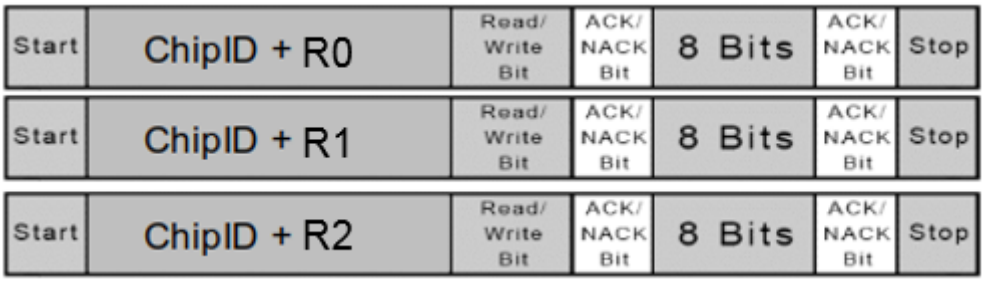


The frame of the I2C protocol is always the same:

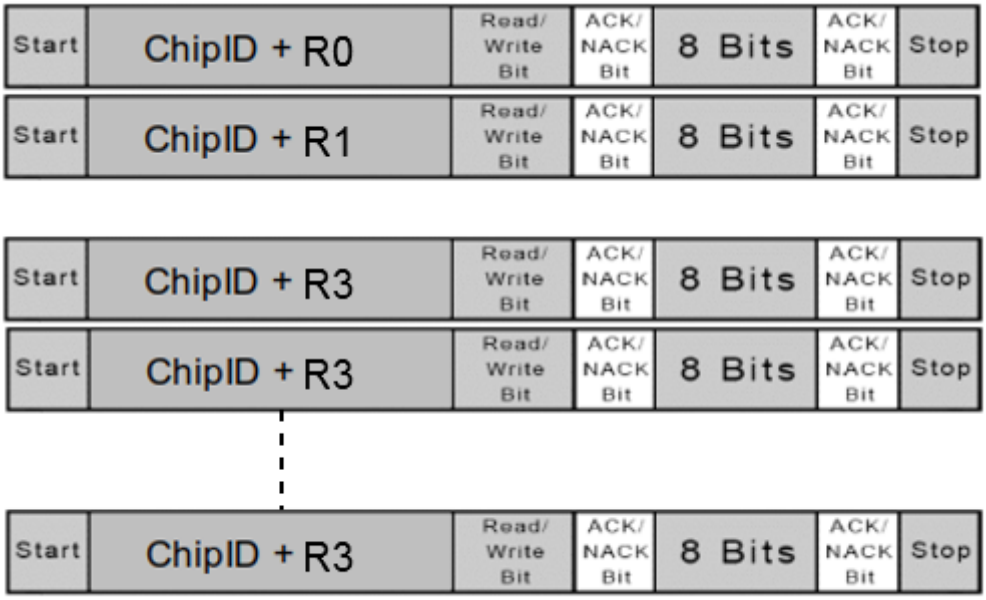


To write, set R/W bit to 0 and to read set R/W to 1.

For instance, to set a specific 8b word of the chip, the users has to write into the R0 register then R1 register to select the good parameters register address, and then write the data into the R2 register.

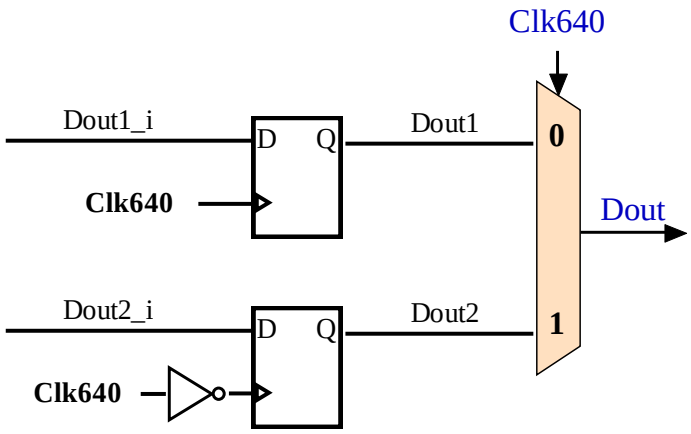


The user can also write into consecutive parameters register addresses: rather to write the parameters into the R2 register, he has to write successively into the R3 register.



1.4.3 Output E-links

The output differential links are composed of a serializer and a driver compatible with the LpGBT protocol. The serializer converts parallel 32 bits words at 40 MHz to a serial train of bits send out at 1280 MHz.



In the table below, the electrical specifications of the driver are given.

Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

The termination load resistor must be placed outside the chip.

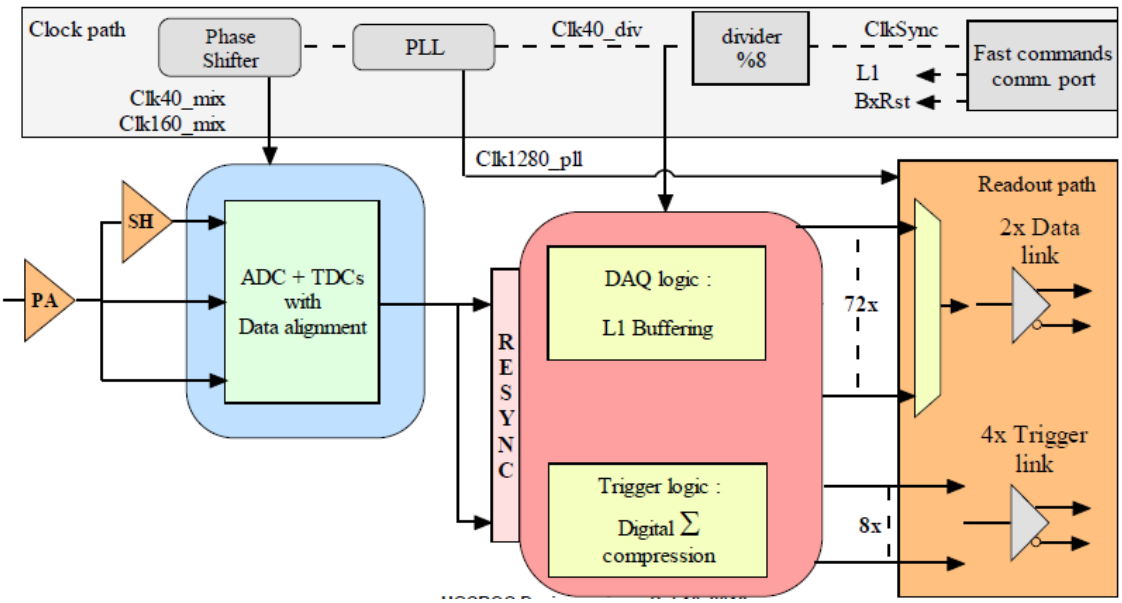
1.5 Ancillary blocks

1.5.1 PLL and clocks distribution

The main specifications of the PLL are described in the following table:

PLL specifications	
Input frequency	40 MHz (LHC bunch clock)
Output frequencies	1.28 GHz and 640, 320, 160 MHz
Jitter cleaner	Low jitter < 15 ps RMS (for an input jitter of 30 ps RMS)
Power consumption	< 2 mW
Area	Pitch 200 µm
Technology	TSMC 130 nm
Temperature	-30 °C

The clock distribution is described in the figure below.



The shaper signal needs to be sampled to its maximum in order to optimize the signal-to-noise ratio; to do that the phase of the 40MHz sampling clock needs to be adjustable. The phase is adjusted by steps of ~ 1.5 ns (640 MHz period).

1.5.2 Bandgap and voltage references

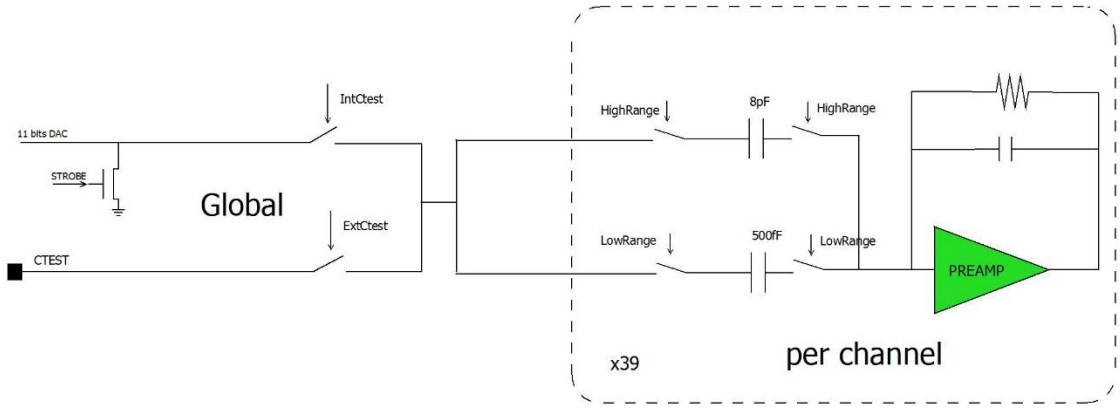
See the document **datasheet_BGP_130nm.pdf** for detailed information about the bandgap.

Four global 10 bits DACs provide voltage references for the analog part: the two discriminator thresholds, the inverted and non-inverted references for the shaper. As the circuit is symmetrical, there are two bandgaps and two sets of voltage references with DACs for the two right and left sub-parts.

The voltage references are fabricated from the bandgap, the 10b DAC and the preamplifier output of a common mode channel (channels CM<1> and CM<3>) so that the chip is not sensitive to the temperature (see Design Review report for more detailed information).

1.5.3 Calibration circuit

The charge injection can be made by injecting a voltage step externally or with an internal 11b-DAC as described in the figure below.

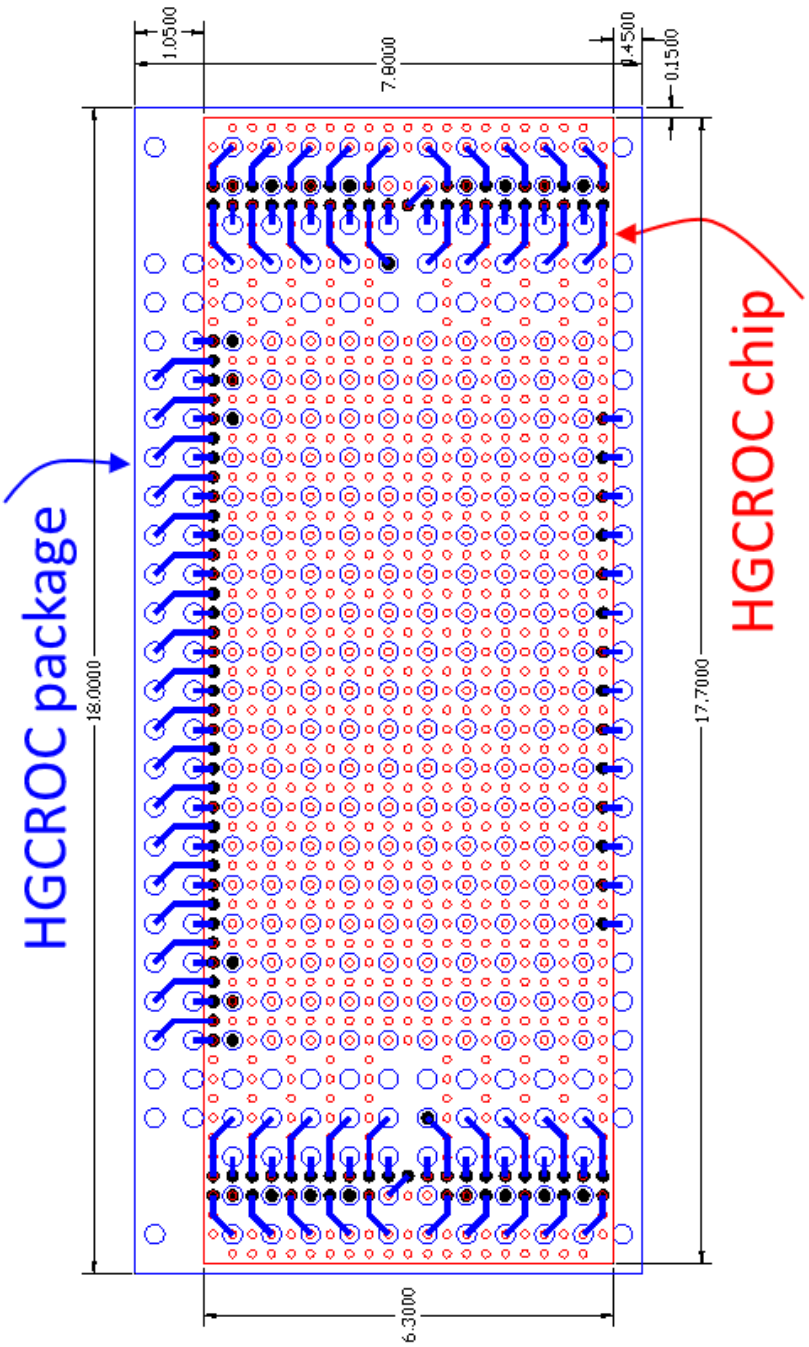


Assuming the 11b-DAC provides a voltage up to around 1 V, the user may set 0.5pF or/and 8pF injection capacitances in the chosen channels, to study the 0 – 0,5 pC range, the 0 – 8 pC range or, by setting the both capacitances, the 0 – 8,5 pC range. To correctly calibrate the ADC/TOT behavior, it is important to have an overlap between the available charge ranges.

The ctest node comes from an external pad and allows the user both to use an external pulser rather than the calibration DAC and also to calibrate the calibration 11b-DAC.

2 Packaging, I/Os and powering scheme

The chip pinout has been defined by the hexaboard constraints [Tommaso et al.] and the BGA package that will be used to house the chips, as shown in figure below.



The two figures below show the left view and the right view of the die. Can be noticed the common column 25 in both figures.

The figure below shows the top view of the BGA map as can be seen on the board.

	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25
A		gnd_dacL	gnd_paL	in<37>	in<36>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	NC	gnddL	sipm_calib	pll_lock	strobe_ext	trig3_n	trig3_p	trig2_n	trig2_p	daq1_n	daq1_p	clk320_p	clk320_n	rstb
B	vssa	vdd_dacL		in<39>	in<38>							vcm_adcL	vdddL	NC	add<3>	NC	add<2>	NC	L1_ext	NC	pll_p	NC	pll_n	NC	error
C	vdd_2v5	gnd_dacL	gnd_paL	in<41>	in<40>	vdd_paL	vdd_skL	vdd_bufL	vdd_adcL	vcm_adcL	vdd_tdcL	gnddL	gnddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	NC
D	vref_skL	NC		in<43>	in<42>							vcm_adcL	vdddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	VHI10	vddd2L	vddd2L	vddd2L	vddd1	vddd1	Resyndoad
E	vdd_2v5	gnd_dacL	gnd_paL	in<45>	in<44>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	gnddL	gnddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	NC
F	vref_noinvL	NC		in<47>	in<46>							vcm_adcL	vdddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	sel_ckext
G	vdd_2v5	gnd_dacL	gnd_paL	in<49>	in<48>	vdd_paL	vdd_skL	vdd_bufL	vdd_adcL	vcm_adcL	vdd_tdcL	gnddL	gnddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	NC
H	vref_invL	NC		in<51>	in<50>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	spare
J	vdd_2v5	gnd_dacL	gnd_paL	in<53>	in<52>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	gnddL	gnddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	NC
K	vref_toaL	vdd_dacL		calib<1>	CM<2>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	spare
L		gnd_dacL	gnd_paL	gnd_paL	gnd_paL	vdd_paL	vdd_skL	vdd_bufL	vdd_adcL	vcm_adcL	vdd_tdcL	gnddL	gnddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	NC
M	vref_totL	vdd_dacL		NC	CM<3>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	spare
N	vdd_2v5	gnd_dacL	gnd_paL	in<54>	in<55>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	gnddL	gnddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	NC
P	vbg_1VL	NC		in<56>	in<57>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	gnd_pll
R	vdd_2v5	gnd_dacL	gnd_paL	in<58>	in<59>	vdd_paL	vdd_skL	vdd_bufL	vdd_adcL	vcm_adcL	vdd_tdcL	gnddL	gnddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	gnd_pll
T	probe_paL	NC		in<60>	in<61>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdd_pll
U	vdd_2v5	gnd_dacL	gnd_paL	in<62>	in<63>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	gnddL	gnddL	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd2L	vddd1	vddd1	vdd_pll
V	in_ctestL	NC		in<64>	in<65>							vcm_adcL	vdddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdd_sc
W	vdd_2v5	gnd_dacL	gnd_paL	in<66>	in<67>	vdd_paL	vdd_skL	vdd_bufL	vdd_adcL	vcm_adcL	vdd_tdcL	gnddL	gnddL	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdd_sc
Y	vssa	vdd_dacL		in<68>	in<69>							vcm_adcL	vdddL	NC	probe_dc1L	NC	probe_dc2L	NC	VHI10L	NC	trig1L	NC	trig2L	NC	NC
Z		gnd_dacL	gnd_paL	in<70>	in<71>	gnd_paL	gnd_skL	gnd_bufL	gnd_adcL	vrefp_adcL	gnd_tdcL	NC	gnddL	NC	VGNL	NC	probe_toaL	NC	probe_totL	NC	adc+L	NC	adc-L	NC	efuse
	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25

25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
rstb	fcmd_p	fcmd_n	daq0_p	daq0_n	trig0_p	trig0_n	trig1_p	trig1_n	sda	scl	i2Crstb	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<0>	in<1>	gnd_paR	gnd_dacR		A
error	NC	clk40_n	NC	clk40_p	NC	ReSync_ext	NC	add<1>	NC	add<0>	NC	vdddR	vcm_adcR							in<2>	in<3>		vdd_dacR	vssa	B
NC	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	gnddR	gnddR	vdd_tdcR	vrefm_adcR	vdd_adcR	vdd_bufR	vdd_skR	vdd_paR	in<4>	in<5>	gnd_paR	gnd_dacR	vdd_2v5	C
Resyncload	vddd1	vddd1	vddd2R	vddd2R	vddd2R	VHI10	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd	vcm_adcR							in<6>	in<7>		vdd_dacR	vref_skR	D
NC	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<8>	in<9>	gnd_paR	gnd_dacR	vdd_2v5	E
sel_ckext	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vdddR	vcm_adcR							in<10>	in<11>		vdd_dacR	vref_noinvR	F
NC	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	gnddR	gnddR	vdd_tdcR	vrefm_adcR	vdd_adcR	vdd_bufR	vdd_skR	vdd_paR	in<12>	in<13>	gnd_paR	gnd_dacR	vdd_2v5	G
spare	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vddd	vcm_adcR							in<14>	in<15>		vdd_dacR	vref_invR	H
NC	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<16>	in<17>	gnd_paR	gnd_dacR	vdd_2v5	J
spare	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdddR	vcm_adcR							CM<0>	calib<0>		vdd_dacR	vref_toaR	K
NC	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	gnddR	gnddR	vdd_tdcR	vrefm_adcR	vdd_adcR	vdd_bufR	vdd_skR	vdd_paR	gnd_pa	gnd_pa	gnd_paR	gnd_dacR	vss	L
spare	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vddd	vcm_adcR							CM<1>	NC		vdd_dacR	vref_totR	M
NC	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<19>	in<18>	gnd_paR	gnd_dacR	vdd_2v5	N
gnd_pll	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdddR	vcm_adcR							in<21>	in<20>		vdd_dacR	vbg_1VR	P
gnd_pll	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	gnddR	gnddR	vdd_tdcR	vrefm_adcR	vdd_adcR	vdd_bufR	vdd_skR	vdd_paR	in<23>	in<22>	gnd_paR	gnd_dacR	vdd_2v5	R
vdd_pll	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vddd	vcm_adcR							in<25>	in<24>		vdd_dacR	probe_paR	T
vdd_pll	vddd1	vddd1	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	vddd2R	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<27>	in<26>	gnd_paR	gnd_dacR	vdd_2v5	U
vdd_sc	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vdddR	vcm_adcR							in<29>	in<28>		vdd_dacR	in_ctestL	V
vdd_sc	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	vss	gnddR	gnddR	vdd_tdcR	vrefm_adcR	vdd_adcR	vdd_bufR	vdd_skR	vdd_paR	in<31>	in<30>	gnd_paR	gnd_dacR	vdd_2v5	W
NC	NC	trig2R	NC	trig1R	NC	VHI10R	NC	probe_dc2R	NC	probe_dc1R	NC	vdddR	vcm_adcR							in<33>	in<32>		vdd_dacR	vssa	Y
efuse	NC	adc-R	NC	adc+R	NC	probe_totR	NC	probe_toaR	NC	VGNR	NC	gnddR	gnddR	gnd_tdc	vrefp_adcR	gnd_adcR	gnd_bufR	gnd_sk	gnd_paR	in<35>	in<34>	gnd_paR	gnd_dacR		Z
25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A		P2V5	P2V5	P2V5	P2V5	P2V5	P2V5	I2C_rst	SDA	Trig1_p	Trig0_p	Daq0_p	Fcmd_p	NC	Clk320_n	Daq1_p	Trig2_p	Trig3_p	Strobe_ext	SiPM_Calib	P2V5	P2V5	P2V5	P2V5	P2V5	P2V5	P2V5	A
B	GND	GND	GND	GND	GND	GND	VrefP_ADC_R	Vcm_ADC_R	SCL	Trig1_n	Trig0_n	Daq0_n	Fcmd_n	Rstb	Clk320_p	Daq1_n	Trig2_n	Trig3_n	PLL_lock	Vcm_ADC_L	VrefP_ADC_L	GND	GND	GND	GND	GND	GND	B
C	GND	IN<1>	IN<3>	IN<2>	IN<0>	GND	VrefN_ADC_R	DVDD	ADD<0>	ADD<1>	ReSync_ext	Clk40_p	Clk40_n	Error	PLL_n	PLL_p	L1_ext	ADD<2>	ADD<3>	DVDD	VrefN_ADC_L	GND	IN<36>	IN<38>	IN<39>	IN<37>	GND	C
D	Vref_SK_R	IN<5>	IN<7>	IN<6>	IN<4>	GND	AVDD_R	DVDD	DVDD	DVDD	VHI	DVDD	DVDD	Resyncload	DVDD	DVDD	VHI	DVDD	DVDD	DVDD	AVDD_L	GND	IN<40>	IN<42>	IN<43>	IN<41>	Vref_SK_L	D
E	Vref_noinv_R	IN<9>	IN<11>	IN<10>	IN<8>	GND	AVDD_R	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	Sel_CK_ext	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD_L	GND	IN<44>	IN<46>	IN<47>	IN<45>	Vref_noinv_L	E
F	Vref_inv_R	IN<13>	IN<15>	IN<14>	IN<12>	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	Spare<1>	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	IN<48>	IN<50>	IN<51>	IN<49>	Vref_inv_L	F
G	Vref_Toa_R	IN<17>	CALIB<0>	CM<0>	IN<16>	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	Spare<2>	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	IN<52>	CM<2>	CALIB<1>	IN<53>	Vref_Toa_L	G
H	Vref_Tot_R	NC	AVDD_0	CM<1>	NC	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	Spare<3>	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	NC	CM<3>	AVDD_1	NC	Vref_Tot_L	H
J	VBG_1V_R	IN<18>	IN<20>	IN<21>	IN<19>	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	GND_PLL	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	IN<55>	IN<57>	IN<56>	IN<54>	VBG_1V_L	J
K	Probe_PA_R	IN<22>	IN<24>	IN<25>	IN<23>	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	VDD_PLL	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	IN<59>	IN<61>	IN<60>	IN<58>	Probe_PA_L	K
L	IN_Ctest_R	IN<26>	IN<28>	IN<29>	IN<27>	GND	AVDD_R	DVDD	VSS	VSS	VSS	VSS	VSS	VDD_SC	VSS	VSS	VSS	VSS	VSS	DVDD	AVDD_L	GND	IN<63>	IN<65>	IN<64>	IN<62>	IN_Ctest_L	L
M	GND	IN<30>	IN<32>	IN<33>	IN<31>	GND	VrefN_ADC_R	DVDD	Probe_DC1_R	Probe_DC2_R	VHI	Trig1_R	Trig2_R	NC	Trig2_L	Trig1_L	VHI	Probe_DC2_L	Probe_DC1_L	DVDD	VrefN_ADC_L	GND	IN<67>	IN<69>	IN<68>	IN<66>	GND	M
N	GND	GND	IN<34>	IN<35>	GND	GND	VrefP_ADC_R	Vcm_ADC_R	VGNR	Probe_Toa_R	Probe_Tot_R	ADCP_R	ADCN_R	EFUSE	ADCN_L	ADCP_L	Probe_Tot_L	Probe_Toa_L	VGNL	Vcm_ADC_L	VrefP_ADC_L	GND	GND	IN<71>	IN<70>	GND	GND	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

2.1 Pin list

	Pin Name	Pin type		Comments	Default value
POWERS/GROUNDS	P2V5	POWER		analog pad ring power supply	1,2V
	AVDD_0	POWER		analog power supply	1,2V
	AVDD_1	POWER		analog power supply	1,2V
	GND	GROUND		analog ground	0V
	DVDD	POWER		digital power supply	1,2V
	VSS	GROUND		digital ground	0V
	VDD_PLL	POWER		PLL power supply	1,2V
	GND_PLL	GROUND		PLL ground	0V
	VDD_SC	POWER		Slow Control power supply	1,2V
	VHI_R	ANALOG		By default keep free ; for monitoring.	1V
	VHI_L	ANALOG		By default keep free ; for monitoring.	1V
Half part (ch. 36 to 71)	Vref_SK_R	ANALOG	Input/Output	Reference voltage of the Sallen-Key amplifier, value close to the preamp input voltage. By default must be kept free. Can be monitored/checked.	200mV
	Vref_noinv_R	ANALOG	Input/Output	Reference voltage of the non-inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_inv_R	ANALOG	Input/Output	Reference voltage of the inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Toa_R	ANALOG	Input/Output	Reference voltage of the TOA threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Tot_R	ANALOG	Input/Output	Reference voltage of the TOT threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	VBG_1V_R	ANALOG	Input/Output	BANDGAP voltage. Value can be tuned by slow-control. Default value = 1V	1V
	Probe_PA_R	ANALOG		preamplifier analog probe. Channel-wise	

	IN_Ctest_R	ANALOG	Input	By default, external pin test, but possibility to connect the calibration DAC output to this pin by slow-control.	
	VrefP_ADC_R	ANALOG	Input/Output	Positive reference voltage of the ADC.	
	VrefN_ADC_R	ANALOG	Input/Output	Negative reference voltage of the ADC.	
	Vcm_ADC_R	ANALOG	Input/Output	Common mode reference voltage of the ADC.	
	Probe_DC1_R	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	Probe_DC2_R	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	VGNR	ANALOG	Input/Output	VGN monitoring	
	Probe_Toa_R	CMOS	Output	TOA discri output probe. Channel-wise	
	Probe_Tot_R	CMOS	Output	TOT discri output probe. Channel-wise	
	Trig1_R	CMOS	Input	External trigger 1	
	Trig2_R	CMOS	Input	External trigger 2	
	ADCP_R	ANALOG	Input/Output	Analog non-inverted probe; positive ADC input	100mV
	ADCN_R	ANALOG	Input/Output	Analog inverted probe; negative ADC input	1,1V
	IN<35:0>	ANALOG	Channel input		200mV
	CALIB<0>	ANALOG	Channel input		200mV
	CM<1:0>	ANALOG	Channel input		200mV
Common pins	I2C_rstb	CMOS	Input	I2C reset; ACTIVE LOW	0V
	SDA	I2C signal		I2C data	
	SCL	I2C clk		I2C clock	
	Error	Open drain		Open collector; external resistor must be added. OR of all the slow-control cells' error signals	
	ADD<3:0>	I2C chip adress		I2C chip address	
	ReSync_ext	CMOS	Input	External ReSync selectable by Slow Control	
	L1_Ext	CMOS	Input	External L1 signal selectable by slow control	
	Strobe_Ext	CMOS	Input	External calibration signal selectable by slow control	
	SiPM_Calib	CMOS	Output	Calibration signal for SiPM	
	ReSyncLoad	CMOS	Input	Serializers synchronization signal	0V
	Sel_CK_ext	CMOS	Input	External 40MHz clock selection (debug purpose); ACTIVE **Low**.	**1.2V**
	Rstb	CMOS	Input	General reset; ACTIVE LOW	
	EFUSE	ANALOG		pin connected to an internal resistor. HGCROC2 => 100Ω. HGCROC2A => 1KΩ. H2GCROC2	

				=> 10KΩ. H2GCROC2A => 100KΩ.	
	PLL_lock	CMOS	Output		
	Clk320_p	CLPS	Input	Fast command 320 MHz clock	
	Clk320_n	CLPS	Input		
	Fcmd_p	CLPS	Input	Fast command data	
	Fcmd_n	CLPS	Input		
	Clk40_p	CLPS	Input	40MHz clock for debug purpose	
	Clk40_n	CLPS	Input		
	PLL_p	CLPS	Output	PLL output probe	
	PLL_n	CLPS	Output		
	Daq0_p	CLPS	Output	Data 0 link	
	Daq0_n	CLPS	Output		
	Daq1_p	CLPS	Output	Data 1 link	
	Daq1_n	CLPS	Output		
	Trig0_p	CLPS	Output	Trigger 0 link	
	Trig0_n	CLPS	Output		
	Trig1_p	CLPS	Output	Trigger 1 link	
	Trig1_n	CLPS	Output		
	Trig2_p	CLPS	Output	Trigger 2 link	
	Trig2_n	CLPS	Output		
	Trig3_p	CLPS	Output	Trigger 3 link	
	Trig3_n	CLPS	Output		
	Spare<3:1>	NC			
Half part (ch. 0 to 35)	Vref_SK_L	ANALOG	Input/Output	Reference voltage of the Sallen-Key amplifier, value close to the preamp input voltage. By default must be kept free. Can be monitored/checked.	200mV
	Vref_noinv_L	ANALOG	Input/Output	Reference voltage of the non-inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_inv_L	ANALOG	Input/Output	Reference voltage of the inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Toa_L	ANALOG	Input/Output	Reference voltage of the TOA threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Tot_L	ANALOG	Input/Output	Reference voltage of the TOT threshold. Value given by an	

				internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	VBG_1V_L	ANALOG	Input/Output	BANDGAP voltage. Value can be tuned by slow-control. Default value = 1V	1V
	Probe_PA_L	ANALOG		preamplifier analog probe. Channel-wise	
	IN_Ctest_L	ANALOG	Input	By default, external pin test, but possibility to connect the calibration DAC output to this pin by slow-control.	
	VrefP_ADC_L	ANALOG	Input/Output	Positive reference voltage of the ADC.	
	VrefN_ADC_L	ANALOG	Input/Output	Negative reference voltage of the ADC.	
	Vcm_ADC_L	ANALOG	Input/Output	Common mode reference voltage of the ADC.	
	Probe_DC1_L	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	Probe_DC2_L	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	VGNL	ANALOG	Input/Output	VGN monitoring	
	Probe_Toa_L	CMOS	Output	TOA discri output probe. Channel-wise	
	Probe_Tot_L	CMOS	Output	TOT discri output probe. Channel-wise	
	Trig1_L	CMOS	Input	External trigger 1	
	Trig2_L	CMOS	Input	External trigger 2	
	ADCP_L	ANALOG	Input/Output	Analog non-inverted probe; positive ADC input	100mV
	ADCN_L	ANALOG	Input/Output	Analog inverted probe; negative ADC input	1,1V
	IN<71:36>	ANALOG	Channel input		200mV
	CALIB<1>	ANALOG	Channel input		200mV
	CM<3:2>	ANALOG	Channel input		200mV

2.2 Short description of some particulars signals/modes

The pin Rstb is the global reset of the chip. This signal is active at 0, it performs the reset of the entire digital part (counters, address pointers), and also of the Master TDC and TDCs, and ADC**. It does not execute the reset of the I2C parameters.**

2.2.1 Fast commands

The fast commands link is composed by two differential links:

- Clk320_(p)(n): Clock at 320 MHz
- Fcmd_(p)(n): fast command as described in section 1.4.1 Fast commands

2.2.2 I2C protocol

The I2C link is composed of four pins

- SDA: I2C data link
- SCL: I2C clock link
- I2C_rstb: reset of the I2C parameters
- Error: Open drain output (a resistor must be routed outside the chip)

2.2.3 Debug and Backup

In the case where Fast Command or PLL do not work properly, the user can configure external clocks and signals to go forward the characterization of the chip.

2.2.3.1 The fast commands and/or 40MHz clock cannot be extracted from the Fcmd link

The available fast commands in HGCROC2 chip are described in the section “1.4.1 Fast Command”. And the parameters allowing to by-pass them are described in “3.7 Top Sub-block I2C parameters”.

If the fast commands cannot be extracted from the Fcmd link, the user can use specific pins to send the commands:

- Strobe_ext in place of the Cmd_Calib command
- L1_ext in place of the Cmd_Trigger command
- OrbitSync_ext in place of the Cmd_Orbit command
- ReSync_ext in place of the Cmd_Sync command

If the 40MHz clock cannot be extracted from the fast command link, the user can set the pin Sel_CK_ext to 0 and use a clock coming from the Clk40_(p)(n) pins. In this debug mode, the fast commands are not provided by the dedicated circuit but by the external pins.

2.2.3.2 The PLL does not work properly

In this case, the user can provide a 640MHz clock via the Clk320 link and by using specific parameters, described in section “3.7 Top Sub-block I2C parameters”, he can provide all necessary clocks (640, 160, 40 MHz).

2.2.4 Calibration

Both in the left and right parts, the Vref_* pins output the reference voltage of the analog front-end. These outputs allows the users to calibrate with an external ADC these references and monitor them as well. In the same way, the value of the bandgap can be tuned and monitored.

The nominal way to calibrate the chip is by sending a Cmd_Calib command via the fast command link. This command send a STROBE signal which performs the injection of the charge given by $CALIB_{DAC}$*RangeCap (see parameters available in the section preamplifier). But the user has also the ability to inject externally a voltage pulse by using a pulser. In this case it has to choose the IN_Ctest_R/L pins (the pin should be externally 50Ω adapted). The IN_Ctest_R/L pins allows also the user to calibrate the $CALIB_{DAC}$, in this case the pin must be in high impedance.

Several pins allows to probe internal signals:

- Probe_PA_R/L: probe the preamplifier output
- Probe_DC1_R/L and Probe_DC3_R/L: probe bias nodes, see parameters of register #8 in ”3.4 Reference Voltage I2C parameters”
    - *Probe 1 (2.5V PAD):*
    - Vbi_pa: “0001”, 500mV default value
    - Vbm_pa: “0010”, 630mV default value

    - Vbm2_pa: “0011”, 420mV default value
    - Vbm3_pa: “0100”, 200mV default value
    - Vbo_pa: “0101”, 400mV default value
    - Vb_inputdac: “0110”, 460mV default value
    - Vb_conv: “0111”, 800mV default value
    - Vb_dac_trim: “1000”, 800mV default value
        - *Probe3 (1.2V PAD):*
    - Vb_suiv2_pa : “1001”
    - Vb_suiv1_pa: “1010”
    - Vbi_discri_tot: : “1011”
    - Probe_Vref_pa: : “1100”
    - Vcp: : “1101”
    - VD_FTDC_N_EXT: : “1110”
    - VD_CTDC_N_EXT: : “1111”
- Probe_DC2_R/L: probe bias nodes, see parameters of register #8 in “3.4 Reference Voltage I2C parameters”
        - *Probe 2 (1.2V):*
    - Vbi_discri_toa: “0001”, 360mV default value
    - Vcasc_discri_toa: “0010”, 1V default value
    - Vbm1_discri_toa: “0011”, 810mV default value
    - Vbm2_discri_toa: “0100”, 800mV default value
    - Vbo_discri_toa: “0101”, 550mV default value
    - EXT_REF_TDC: “0110”,
    - NC: “0111”
    - NC : “1000”
    - NC : “1001”
    - Vbm_discri_tot: “1010”
    - Vbo_discri_tot: “1011”
    - Probe_Vref_time: “1100”
    - Vcn: “1101”
    - VD_FTDC_P_EXT: “1110”,
    - VD_CTDC_P_EXT: “1111”,
- Probe_Toa_R/L: probe the TOA discriminator output
- Probe_Tot_R/L: probe the TOT discriminator output
- ADCP_R/L: probe the non_inverted shaper output; allows also to calibrate the ADCs by applying a DC voltage
- ADCN_R/L: probe the inverted shaper output; allows also to calibrate the ADCs by applying a DC voltage
- Trig_R/L and Trig2_R/L: allows to applying an external pulse to the discriminators, TOT and/or TOA, in order to calibrate the TDCs.
- VrefP_ADC_R/L: positive reference voltage of the ADC
- VrefN_ADC_R/L: negative reference voltage of the ADC. On the half (ch 36-71), connected to Vcm_ADC as negative reference on this side is the ADC ground.
- Vcm_ADC_R/L: common mode reference of the ADC

3 ASIC parameters

As described in section **1.4.2 I2C,** the I2C circuit has 8 internal registers; the four first are dedicated to write/read the slow-control parameters. Registers 4, 5 and 6 are direct access registers and the register 7 is a status register in read-only mode.

In the tables below, the content of the direct access registers is described.

I2C Register R4			
Bit	**Name**	**Default**	**Description**
0	AutoReload	"0"	Allows to rewrite the value after a SEU
1	EdgeSel	"0"	Selection of the clock edge of the 320MHz clock
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

I2C Register R5			
Bit	**Name**	**Default**	**Description**
0	NA	"0"	
1	NA	"0"	
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

I2C Register R6			
Bit	**Name**	**Default**	**Description**
0	NA	"0"	
1	NA	"0"	
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

I2C Register R7 (Status , read only)			
Bit	**Name**	**Default**	**Description**
0	Error		OR of all the slow-control cells' error signals
1	Parity		Parity of all the slow-control cells' values
2	Pll_Lock		Pll lock flag. "1" pll is locked
3	NA		

4	NA		
5	NA		
6	NA		
7	NA		

3.1 I2C Addressing

The four first I2C registers, R0-3, allow to define the address and the data to write or read into the internal 8 bits registers distributed into the chip sub-parts. R0 and R1 define the address of internal 8 bits registers. R2 defines the data to write into the chosen internal 8 bits register. R3 allows the user to access successive register address.

The chip, from I2C protocol point of view, is divided in sub-blocks containing maximum 32 registers each. In consequence, the address in 16 bits (given in R0 and R1) is composed of two sub-address:

- The 11 MSB bits code the address of the sub-block
- The 5 LSB bits code the address of the register of the sub-block

The table below gives the address, the name and a short description of all the sub-blocks.

Sub-block name	Sub-block address	Description
Channel_0	261	Registers described in "**channel wise**" I2C parameters section
Channel_1	260	
Channel_2	259	
Channel_3	258	
Channel_4	265	
Channel_5	264	
Channel_6	263	
Channel_7	262	
Channel_8	269	
Channel_9	268	
Channel_10	267	
Channel_11	266	
Channel_12	273	
Channel_13	272	
Channel_14	271	
Channel_15	270	
Channel_16	294	
Channel_17	256	
Channel_18	277	
CM1	276	
CM0	275	
CALIB0	274	
Channel_19	295	
Channel_20	278	

Channel_21	279	
Channel_22	280	
Channel_23	281	
Channel_24	282	
Channel_25	283	
Channel_26	284	
Channel_27	285	
Channel_28	286	
Channel_29	287	
Channel_30	288	
Channel_31	289	
Channel_32	290	
Channel_33	291	
Channel_34	292	
Channel_35	293	
Reference Voltage 0	296	Registers described in "**Reference Voltage**" section
Global Analog 0	297	Registers described in "**Global analog**" section
Master TDC 0	298	Registers described in "**Master TDC**" section
Digital Half 0	299	Registers described in "**Digital half**" section
No Register		
Channel_36	5	Registers described in "**channel wise**" I2C parameters section
Channel_37	4	
Channel_38	3	
Channel_39	2	
Channel_40	9	
Channel_41	8	
Channel_42	7	
Channel_43	6	
Channel_44	13	
Channel_45	12	
Channel_46	11	
Channel_47	10	
Channel_48	17	
Channel_49	16	
Channel_50	15	
Channel_51	14	
Channel_52	38	
Channel_53	0	
Channel_54	21	
CM3	20	
CM2	19	

CALIB1	18	
Channel_55	39	
Channel_56	22	
Channel_57	23	
Channel_58	24	
Channel_59	25	
Channel_60	26	
Channel_61	27	
Channel_62	28	
Channel_63	29	
Channel_64	30	
Channel_65	31	
Channel_66	32	
Channel_67	33	
Channel_68	34	
Channel_69	35	
Channel_70	36	
Channel_71	37	
Reference Voltage 1	40	Registers described in "**Reference Voltage**" section
Global Analog 1	41	Registers described in "**Global analog**" section
Master TDC 1	42	Registers described in "**Master TDC**" section
Digital Half 1	43	Registers described in "**Digital half**" section
Top	44	Registers described in "**Top sub-block**" section

3.2 "Channel-wise" I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	Inputdac<0>	"1"	Input DAC value
1	Inputdac<1>	"1"	
2	Inputdac<2>	"1"	
3	Inputdac<3>	"1"	
4	Inputdac<4>	"1"	
5	Inputdac<5>	"0"	
6	Dacb<4>	"1"	DC current trimming DAC (MSB-1, MSB)
7	Dacb<5>	"1"	

Register # 1			
Bit	**Name**	**Default**	**Description**
0	Sign_dac	“0”	DC current trimming DAC sign
1	Ref_dac_toa<0>	“0”	Local 5b-DAC for TOA threshold tuning
2	Ref_dac_toa<1>	“0”	
3	Ref_dac_toa<2>	“0”	
4	Ref_dac_toa<2>	“0”	
5	Ref_dac_toa<4>	“0”	
6	Dacb<2>	“1”	DC current trimming DAC (MSB-2, MSB-3)
7	Dacb<3>	“1”	

Register # 2			
Bit	**Name**	**Default**	**Description**
0	Probe_noinv	“0”	Non inverter shaper output probe (“1” = selected)
1	Ref_dac_tot<0>	“0”	Local 5b-DAC for TOT threshold tuning
2	Ref_dac_tot<1>	“0”	
3	Ref_dac_tot<2>	“0”	
4	Ref_dac_tot<3>	“0”	
5	Ref_dac_tot<4>	“0”	
6	Dacb<0>	“1”	DC current trimming DAC (LSB, LSB+1)
7	Dacb<1>	“1”	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	Mask_toa	“0”	TOA discri output mask (“1” = masked)
1	Ref_dac_inv<0>	“0”	Local 5b-DAC for ADC pedestal tuning
2	Ref_dac_inv<1>	“0”	
3	Ref_dac_inv<2>	“0”	
4	Ref_dac_inv<3>	“0”	
5	Ref_dac_inv<4>	“0”	
6	Sel_trigger_toa	“0”	External trigger selection for TOA (“0” = Ext Trig1; “1” = Ext Trig2)
7	Probe_inv	“0”	Inverter shaper output probe (“1” = selected)

Register # 4			
Bit	**Name**	**Default**	**Description**
0	Probe_pa	“0”	Preamplifier output probe
1	LowRange	“0”	0.5pF injection cap
2	HighRange	“0”	8pF injection cap
3	Channel_off	“0”	“1” = preamplifier input tied to ground
4	Sel_trigger_tot	“0”	External trigger selection for TOT (“0” = Ext Trig1; “1” = Ext Trig2)
5	Mask_tot	“0”	TOT discri output mask (“1” = masked)
6	Probe_tot	“0”	TOT discri output probe
7	Probe_toa	“0”	TOA discri output probe

Register # 5			
Bit	**Name**	**Default**	**Description**
0	DAC_CAL_FTDC_TOA<0>	"0"	Tune the fine gain of the TOA FTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
1	DAC_CAL_FTDC_TOA<1>	"0"	
2	DAC_CAL_FTDC_TOA<2>	"0"	
3	DAC_CAL_FTDC_TOA<3>	"0"	
4	DAC_CAL_FTDC_TOA<4>	"0"	
5	DAC_CAL_FTDC_TOA<5>	"0"	
6	NA	"0"	
7	Mask_adc	"0"	"1" = ADC clock off

Register # 6			
Bit	**Name**	**Default**	**Description**
0	DAC_CAL_CTDC_TOA<0>	"0"	Tune the fine gain of the TOA CTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
1	DAC_CAL_CTDC_TOA<1>	"0"	
2	DAC_CAL_CTDC_TOA<2>	"0"	
3	DAC_CAL_CTDC_TOA<3>	"0"	
4	DAC_CAL_CTDC_TOA<4>	"0"	
5	DAC_CAL_CTDC_TOA<5>	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	DAC_CAL_FTDC_TOT<0>	"0"	Tune the fine gain of the TOA FTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
1	DAC_CAL_FTDC_TOT<1>	"0"	
2	DAC_CAL_FTDC_TOT<2>	"0"	
3	DAC_CAL_FTDC_TOT<3>	"0"	
4	DAC_CAL_FTDC_TOT<4>	"0"	
5	DAC_CAL_FTDC_TOT<5>	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 8			
Bit	**Name**	**Default**	**Description**
0	DAC_CAL_CTDC_TOT<0>	"0"	Tune the fine gain of the TOT CTDC: 5 bits DAC <0:4> (1kΩ x 32) by the BIAS_CAL_DAC_P and the sign 1 bit <5> VD_P CAL = VD_P + (sign <5> x <0:4> x 1kΩ x BIAS_CAL_DAC_P)
1	DAC_CAL_CTDC_TOT<1>	"0"	
2	DAC_CAL_CTDC_TOT<2>	"0"	
3	DAC_CAL_CTDC_TOT<3>	"0"	
4	DAC_CAL_CTDC_TOT<4>	"0"	
5	DAC_CAL_CTDC_TOT<5>	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 9			
Bit	**Name**	**Default**	**Description**
0	IN_FTDC_ENCODER_TOA<0>	"0"	

1	IN_FTDC_ENCODER_TOA<1>	"0"	Adjust the ToA FTDC offset by 5 bits <0:4> and the sign 1 bit <5> OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
2	IN_FTDC_ENCODER_TOA<2>	"0"	
3	IN_FTDC_ENCODER_TOA<3>	"0"	
4	IN_FTDC_ENCODER_TOA<4>	"0"	
5	IN_FTDC_ENCODER_TOA<5>	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 10			
Bit	**Name**	**Default**	**Description**
0	IN_FTDC_ENCODER_TOT<0>	"0"	Adjust the ToT FTDC offset by 5 bits <0:4> and the sign 1 bit <5> OFFSET = FTDC_TDC<0:5> + (sign <5> x DATA<0:4>)
1	IN_FTDC_ENCODER_TOT<1>	"0"	
2	IN_FTDC_ENCODER_TOT<2>	"0"	
3	IN_FTDC_ENCODER_TOT<3>	"0"	
4	IN_FTDC_ENCODER_TOT<4>	"0"	
5	IN_FTDC_ENCODER_TOT<5>	"0"	
6	NA	"0"	
7	DIS_TDC	"0"	"1" = TDC clocks off

Register # 11			
Bit	**Name**	**Default**	**Description**
0	ExtData<8>	"0"	Forced ADC data, bits 9 & 8
1	ExtData<9>	"0"	
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	Mask_AlignBuffer	"0"	"1" = AlignBuffer clock off

Register # 12			
Bit	**Name**	**Default**	**Description**
0	Adc_pedestal<0>	"0"	ADC pedestal value
1	Adc_pedestal<1>	"0"	
2	Adc_pedestal<2>	"0"	
3	Adc_pedestal<3>	"0"	
4	Adc_pedestal<4>	"0"	
5	Adc_pedestal<5>	"0"	
6	Adc_pedestal<6>	"0"	
7	Adc_pedestal<7>	"0"	

Register # 13			
Bit	**Name**	**Default**	**Description**
0	ExtData<0>	"0"	Forced ADC data, bits 7 downto 0
1	ExtData<1>	"0"	
2	ExtData<2>	"0"	
3	ExtData<3>	"0"	

4	ExtData<4>	“0”	
5	ExtData<5>	“0”	
6	ExtData<6>	“0”	
7	ExtData<7>	“0”	

3.3 “Global analog” I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	ON_dac_trim	“1”	“1” = enable DC trimming bias
1	ON_input_dac	“1”	“1” = enable input DAC bias
2	ON_conv	“1”	“1” = enable conveyor bias
3	ON_pa	“1”	“1” = enable preamp bias
4	Gain_conv<0>	“0”	Conveyor Gain: **<0> = 0.025, <1> = 0.05, <2> = 0.1, <3> = 0.2**
5	Gain_conv<1>	“0”	
6	Gain_conv<2>	“1”	
7	Gain_conv<3>	“0”	

Register # 1			
Bit	**Name**	**Default**	**Description**
0	ON_rtr	“1”	“1” = enable shaper amplifiers bias
1	Sw_super_conv	“1”	“1” = enable “super conveyor”
2	Dacb_vb_conv<0>	“1”	6b-DAC for conveyor current tuning
3	Dacb_vb_conv<1>	“1”	
4	Dacb_vb_conv<2>	“0”	
5	Dacb_vb_conv<3>	“0”	
6	Dacb_vb_conv<4>	“1”	
7	Dacb_vb_conv<5>	“1”	

Register # 2			
Bit	**Name**	**Default**	**Description**
0	ON_toa	“1”	“1” = enable TOA discri bias
1	ON_tot	“1”	“1” = enable TOT discri bias
2	Dacb_vbi_pa<0>	“1”	6b-DAC for preamp input stage current tuning
3	Dacb_vbi_pa<1>	“1”	
4	Dacb_vbi_pa<2>	“1”	
5	Dacb_vbi_pa<3>	“1”	
6	Dacb_vbi_pa<4>	“1”	
7	Dacb_vbi_pa<5>	“0”	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	Ibi_sk<0>	“0”	S-K amplifier input stage current
1	Ibi_sk<1>	“0”	
2	Ibo_sk<0>	“0”	S-K amplifier output stage current
3	Ibo_sk<1>	“1”	

4	Ibo_sk<2>	“0”	
5	Ibo_sk<3>	“1”	
6	Ibo_sk<4>	“0”	
7	Ibo_sk<5>	“0”	

Register # 4			
Bit	**Name**	**Default**	**Description**
0	Ibi_inv<0>	“0”	Inverter amplifier input stage current
1	Ibi_inv<1>	“0”	
2	Ibo_inv<0>	“0”	Inverter amplifier output stage current
3	Ibo_inv<1>	“1”	
4	Ibo_inv<2>	“0”	
5	Ibo_inv<3>	“1”	
6	Ibo_inv<4>	“0”	
7	Ibo_inv<5>	“0”	

Register # 5			
Bit	**Name**	**Default**	**Description**
0	Ibi_noinv<0>	“0”	Non Inverter amplifier input stage current
1	Ibi_noinv<1>	“0”	
2	Ibo_noinv<0>	“0”	Non Inverter amplifier output stage current
3	Ibo_noinv<1>	“1”	
4	Ibo_noinv<2>	“0”	
5	Ibo_noinv<3>	“1”	
6	Ibo_noinv<4>	“0”	
7	Ibo_noinv<5>	“0”	

Register # 6			
Bit	**Name**	**Default**	**Description**
0	Ibi_inv_buf<0>	“1”	Inverter buffer input stage current
1	Ibi_inv_buf<1>	“1”	
2	Ibo_inv_buf<0>	“0”	Inverter buffer output stage current
3	Ibo_inv_buf<1>	“1”	
4	Ibo_inv_buf<2>	“1”	
5	Ibo_inv_buf<3>	“0”	
6	Ibo_inv_buf<4>	“0”	
7	Ibo_inv_buf<5>	“1”	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	Ibi_noinv_buf<0>	“1”	Non Inverter buffer input stage current
1	Ibi_noinv_buf<1>	“1”	
2	Ibo_noinv_buf<0>	“0”	Non Inverter buffer output stage current
3	Ibo_noinv_buf<1>	“1”	
4	Ibo_noinv_buf<2>	“1”	
5	Ibo_noinv_buf<3>	“0”	
6	Ibo_noinv_buf<4>	“0”	

7	Ibo_noinv_buf<5>	“1”	

Register # 8			
Bit	**Name**	**Default**	**Description**
0	Sw_cd<0>	“1”	Internal capacitors in // : <0>=5pF; <1>=10pF; <2>=20pF
1	Sw_cd<1>	“1”	
2	Sw_cd<2>	“1”	
3	En_hyst_tot	“0”	“1” = enable the TOT discri hysteresis
4	Sw_Cf_comp<0>	“0”	Preamp feedback comp. cap. <0> = 50fF; <1> = 100fF; <2> = 200fF; <3> = 400fF
5	Sw_Cf_comp<1>	“1”	
6	Sw_Cf_comp<2>	“0”	
7	Sw_Cf_comp<3>	“1”	

Register # 9			
Bit	**Name**	**Default**	**Description**
0	Sw_Cf<0>	“0”	Preamp feedback. cap. <0> = 50fF; <1> = 100fF; <2> = 200fF; <3> = 400fF
1	Sw_Cf<1>	“1”	
2	Sw_Cf<2>	“0”	
3	Sw_Cf<3>	“1”	
4	Sw_Rf<0>	“0”	Preamp feedback Res. <0> = 10K, <1> = 15K, <2> = 20K, <3> = 25K In //
5	Sw_Rf<1>	“0”	
6	Sw_Rf<2>	“0”	
7	Sw_Rf<3>	“1”	

Register # 10			
Bit	**Name**	**Default**	**Description**
0	NA	“0”	
1	Clr_ShaperTail	“0”	
2	SelRisingEdge	“1”	“1” = AlignBuffer provides data on rising edge
3	SelExtADC	“0”	“1” = Forced ADC data send to the DRAM
4	Clr_ADC	“0”	
5	S_sk<0>	“0”	S-K amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
6	S_sk<1>	“1”	
7	S_sk<2>	“0”	

Register # 11			
Bit	**Name**	**Default**	**Description**
0	NA	“0”	
1	NA	“0”	
2	S_inv<0>	“0”	Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
3	S_inv<1>	“1”	
4	S_inv<2>	“0”	
5	S_noinv<0>	“0”	Non Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
6	S_noinv<1>	“1”	
7	S_noinv<2>	“0”	

Register # 12			
Bit	**Name**	**Default**	**Description**
0	NA	"0"	
1	NA	"0"	
2	S_inv_buf<0>	"0"	Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
3	S_inv_buf<1>	"1"	
4	S_inv_buf<2>	"1"	
5	S_noinv_buf<0>	"0"	Non Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
6	S_noinv_buf<1>	"1"	
7	S_noinv_buf<2>	"1"	

Register # 13			
Bit	**Name**	**Default**	**Description**
0	Ref_adc<0>	"0"	Input stage current of the Ref ADC OTA
1	Ref_adc<1>	"0"	
2	Delay40<0>	"0"	Delay tuning for bits <4:0> "000" = faster conversion
3	Delay40<1>	"0"	
4	Delay40<2>	"0"	
5	Delay65<0>	"0"	Delay tuning for bits <6:5> "000" = faster conversion
6	Delay65<1>	"0"	
7	Delay65<2>	"0"	

Register # 14			
Bit	**Name**	**Default**	**Description**
0	ON_ref_adc	"1"	"1" = enable ADC ref OTA
1	Pol_adc	"1"	ADC input swap
2	Delay87<0>	"0"	Delay tuning for bits <8:7> "000" = faster conversion
3	Delay87<1>	"0"	
4	Delay87<2>	"0"	
5	Delay9<0>	"0"	Delay tuning for bit <9> "000" = faster conversion
6	Delay9<1>	"0"	
7	Delay9<2>	"0"	

3.4 "Reference Voltage" I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	Probe_vref_pa	"0"	10b-DAC ref probe
1	Probe_vref_time	"0"	10b-DAC ref probe
2	Refi<0>	"1"	Bandgap current tuning
3	Refi<1>	"1"	
4	Vbg_1v<0>	"1"	1V bandgap ref. tuning
5	Vbg_1v<1>	"1"	
6	Vbg_1v<2>	"1"	
7	ON_dac	"1"	"1" = enable DACs

Register # 1			
Bit	**Name**	**Default**	**Description**
0	Noinv_vref<0>	“0”	
1	Noinv_vref<1>	“0”	
2	Inv_vref<0>	“0”	
3	Inv_vref<1>	“0”	
4	Toa_vref<0>	“0”	
5	Toa_vref<1>	“0”	
6	Tot_vref<0>	“0”	
7	Tot_vref<1>	“0”	

Register # 2			
Bit	**Name**	**Default**	**Description**
0	Tot_vref<2>	“0”	TOT threshold global value
1	Tot_vref<3>	“0”	
2	Tot_vref<4>	“1”	
3	Tot_vref<5>	“1”	
4	Tot_vref<6>	“0”	
5	Tot_vref<7>	“1”	
6	Tot_vref<8>	“1”	
7	Tot_vref<9>	“0”	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	Toa _vref<2>	“0”	TOA threshold global value
1	Toa _vref<3>	“0”	
2	Toa _vref<4>	“1”	
3	Toa _vref<5>	“1”	
4	Toa _vref<6>	“1”	
5	Toa _vref<7>	“0”	
6	Toa _vref<8>	“0”	
7	Toa _vref<9>	“0”	

Register # 4			
Bit	**Name**	**Default**	**Description**
0	Inv_vref<2>	“0”	Inverter shaper global reference
1	Inv_vref<3>	“0”	
2	Inv_vref<4>	“0”	
3	Inv_vref<5>	“0”	
4	Inv_vref<6>	“0”	
5	Inv_vref<7>	“1”	
6	Inv_vref<8>	“1”	
7	Inv_vref<9>	“0”	

Register # 5			
Bit	**Name**	**Default**	**Description**

0	Noinv_vref<2>	“1”	Non Inverter shaper global reference
1	Noinv_vref<3>	“1”	
2	Noinv_vref<4>	“1”	
3	Noinv_vref<5>	“1”	
4	Noinv_vref<6>	“0”	
5	Noinv_vref<7>	“0”	
6	Noinv_vref<8>	“1”	
7	Noinv_vref<9>	“0”	

Register # 6			
Bit	**Name**	**Default**	**Description**
0	Calib_dac<0>	“0”	Calibration DAC value
1	Calib_dac<1>	“0”	
2	Calib_dac<2>	“0”	
3	Calib_dac<3>	“0”	
4	Calib_dac<4>	“0”	
5	Calib_dac<5>	“0”	
6	Calib_dac<6>	“0”	
7	Calib_dac<7>	“0”	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	Calib_dac<8>	“0”	Calibration DAC value
1	Calib_dac<9>	“0”	
2	Calib_dac<10>	“0”	
3	Calib_dac<11>	“0”	
4	NA	“0”	
5	NA	“0”	
6	IntCtest	“0”	Selection of the Calibration DAC
7	ExtCtest	“0”	Selection of the external pulse test

Register # 8			
Bit	**Name**	**Default**	**Description**
0	Probe_dc<0>	“0”	Selection of the probe_dc1 and probe_dc3
1	Probe_dc<1>	“0”	
2	Probe_dc<2>	“0”	
3	Probe_dc<3>	“0”	
4	Probe_dc<4>	“0”	Selection of the probe_dc2
5	Probe_dc<5>	“0”	
6	Probe_dc<6>	“0”	
7	Probe_dc<7>	“0”	

3.5 “Master TDC” I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_TA_SELECT_GAIN_TOA<0>	“1”	
1	GLOBAL_TA_SELECT_GAIN_TOA<1>	“1”	
2	GLOBAL_TA_SELECT_GAIN_TOA<2>	“0”	
3	GLOBAL_TA_SELECT_GAIN_TOA<3>	“0”	
4	GLOBAL_TA_SELECT_GAIN_TOT<0>	“1”	
5	GLOBAL_TA_SELECT_GAIN_TOT<1>	“1”	
6	GLOBAL_TA_SELECT_GAIN_TOT<2>	“0”	
7	GLOBAL_TA_SELECT_GAIN_TOT<3>	“0”	

Register # 1			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_MODE_NO_TOT_SUB	“0”	
1	GLOBAL_LATENCY_TIME<0>	“0”	
2	GLOBAL_LATENCY_TIME<1>	“1”	
3	GLOBAL_LATENCY_TIME<2>	“0”	
4	GLOBAL_LATENCY_TIME<3>	“1”	
5	GLOBAL_MODE_FTDC_TOA_S0	“0”	
6	GLOBAL_MODE_FTDC_TOA_S1	“1”	
7	GLOBAL_SEU_TIME_OUT	“1”	

Register # 2			
Bit	**Name**	**Default**	**Description**
0	BIAS_FOLLOWER_CAL_P_D<0>	“0”	
1	BIAS_FOLLOWER_CAL_P_D<1>	“0”	
2	BIAS_FOLLOWER_CAL_P_D<2>	“0”	
3	BIAS_FOLLOWER_CAL_P_D<3>	“0”	
4	BIAS_FOLLOWER_CAL_P_EN	“0”	
5	INV_FRONT_40MHZ	“0”	
6	START_COUNTER	“1”	
7	CALIB_CHANNEL_DLL	“0”	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	VD_CTDC_P_D<0>	“0”	
1	VD_CTDC_P_D<1>	“0”	
2	VD_CTDC_P_D<2>	“0”	
3	VD_CTDC_P_D<3>	“0”	
4	VD_CTDC_P_D<4>	“0”	
5	VD_CTDC_P_DAC_EN	“0”	
6	EN_MASTER_CTDC_VOUT_INIT	“0”	
7	EN_MASTER_CTDC_DLL	“1”	

Register # 4			
Bit	**Name**	**Default**	**Description**
0	BIAS_CAL_DAC_CTDC_P_D<0>	“0”	

1	BIAS_CAL_DAC_CTDC_P_D<1>	“0”	
2	CTDC_CALIB_FREQUENCY<0>	“0”	
3	CTDC_CALIB_FREQUENCY<1>	“1”	
4	CTDC_CALIB_FREQUENCY<2>	“0”	
5	CTDC_CALIB_FREQUENCY<3>	“0”	
6	CTDC_CALIB_FREQUENCY<4>	“0”	
7	CTDC_CALIB_FREQUENCY<5>	“0”	

Register # 5			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_MODE_TOA_DIRECT_OUTPUT	“0”	
1	BIAS_I_CTDC_D<0>	“0”	
2	BIAS_I_CTDC_D<1>	“0”	
3	BIAS_I_CTDC_D<2>	“0”	
4	BIAS_I_CTDC_D<3>	“1”	
5	BIAS_I_CTDC_D<4>	“1”	
6	BIAS_I_CTDC_D<5>	“0”	
7	FOLLOWER_CTDC_EN	“1”	

Register # 6			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_EN_BUFFER_CTDC	“0”	
1	VD_CTDC_N_FORCE_MAX	“1”	
2	VD_CTDC_N_D<0>	“0”	
3	VD_CTDC_N_D<1>	“0”	
4	VD_CTDC_N_D<2>	“0”	
5	VD_CTDC_N_D<3>	“0”	
6	VD_CTDC_N_D<4>	“0”	
7	VD_CTDC_N_DAC_EN	“0”	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	CTRL_IN_REF_CTDC_P_D<0>	“0”	
1	CTRL_IN_REF_CTDC_P_D<0>	“0”	
2	CTRL_IN_REF_CTDC_P_D<0>	“0”	
3	CTRL_IN_REF_CTDC_P_D<0>	“0”	
4	CTRL_IN_REF_CTDC_P_D<0>	“0”	
5	CTRL_IN_REF_CTDC_P_EN	“0”	
6	BIAS_CAL_DAC_CTDC_P_D<2>	“0”	
7	BIAS_CAL_DAC_CTDC_P_D<3>	“0”	

Register # 8			
Bit	**Name**	**Default**	**Description**
0	CTRL_IN_SIG_CTDC_P_D<0>	“0”	
1	CTRL_IN_SIG_CTDC_P_D<1>	“0”	
2	CTRL_IN_SIG_CTDC_P_D<2>	“0”	
3	CTRL_IN_SIG_CTDC_P_D<3>	“0”	

4	CTRL_IN_SIG_CTDC_P_D<4>	“0”	
5	CTRL_IN_SIG_CTDC_P_EN	“0”	
6	GLOBAL_INIT_DAC_B_CTDC	“0”	
7	BIAS_CAL_DAC_CTDC_P_EN	“0”	

Register # 9			
Bit	**Name**	**Default**	**Description**
0	VD_FTDC_P_D<0>	“0”	
1	VD_FTDC_P_D<1>	“0”	
2	VD_FTDC_P_D<2>	“0”	
3	VD_FTDC_P_D<3>	“0”	
4	VD_FTDC_P_D<4>	“0”	
5	VD_FTDC_P_DAC_EN	“0”	
6	EN_MASTER_FTDC_VOUT_INIT	“0”	
7	EN_MASTER_FTDC_DLL	“1”	

Register # 10			
Bit	**Name**	**Default**	**Description**
0	BIAS_CAL_DAC_FTDC_P_D<0>	“0”	
1	BIAS_CAL_DAC_FTDC_P_D<1>	“0”	
2	FTDC_CALIB_FREQUENCY<0>	“0”	
3	FTDC_CALIB_FREQUENCY<1>	“1”	
4	FTDC_CALIB_FREQUENCY<2>	“0”	
5	FTDC_CALIB_FREQUENCY<3>	“0”	
6	FTDC_CALIB_FREQUENCY<4>	“0”	
7	FTDC_CALIB_FREQUENCY<5>	“0”	

Register # 11			
Bit	**Name**	**Default**	**Description**
0	EN_REF_BG	“1”	
1	BIAS_I_FTDC_D<0>	“0”	
2	BIAS_I_FTDC_D<1>	“0”	
3	BIAS_I_FTDC_D<2>	“0”	
4	BIAS_I_FTDC_D<3>	“1”	
5	BIAS_I_FTDC_D<4>	“1”	
6	BIAS_I_FTDC_D<5>	“0”	
7	FOLLOWER_FTDC_EN	“1”	

Register # 12			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_EN_BUFFER_FTDC	“0”	
1	VD_FTDC_N_FORCE_MAX	“1”	
2	VD_FTDC_N_D<0>	“0”	
3	VD_FTDC_N_D<1>	“0”	
4	VD_FTDC_N_D<2>	“0”	
5	VD_FTDC_N_D<3>	“0”	
6	VD_FTDC_N_D<4>	“0”	

7	VD_FTDC_N_DAC_EN	“0”	

Register # 13			
Bit	**Name**	**Default**	**Description**
0	CTRL_IN_SIG_FTDC_P_D<0>	“0”	
1	CTRL_IN_SIG_FTDC_P_D<1>	“0”	
2	CTRL_IN_SIG_FTDC_P_D<2>	“0”	
3	CTRL_IN_SIG_FTDC_P_D<3>	“0”	
4	CTRL_IN_SIG_FTDC_P_D<4>	“0”	
5	CTRL_IN_SIG_FTDC_P_EN	“0”	
6	GLOBAL_INIT_DAC_B_FTDC	“0”	
7	BIAS_CAL_DAC_FTDC_P_EN	“0”	

Register # 14			
Bit	**Name**	**Default**	**Description**
0	CTRL_IN_REF_FTDC_P_D<0>	“0”	
1	CTRL_IN_REF_FTDC_P_D<1>	“0”	
2	CTRL_IN_REF_FTDC_P_D<2>	“0”	
3	CTRL_IN_REF_FTDC_P_D<3>	“0”	
4	CTRL_IN_REF_FTDC_P_D<4>	“0”	
5	CTRL_IN_REF_FTDC_P_EN	“0”	
6	BIAS_CAL_DAC_FTDC_P_D<2>	“0”	
7	BIAS_CAL_DAC_FTDC_P_D<3>	“0”	

Register # 15			
Bit	**Name**	**Default**	**Description**
0	GLOBAL_DISABLE_TOT_LIMIT	“0”	
1	GLOBAL_FORCE_EN_CLK	“0”	
2	GLOBAL_FORCE_EN_OUTPUT_DATA	“0”	
3	GLOBAL_FORCE_EN_TOT	“0”	
4	NA	“0”	
5	NA	“0”	
6	NA	“0”	
7	NA	“0”	

See Annexe A for more details about TDCs parameters.

3.6 “Digital half” I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	SelRawData	“1”	“1” = send raw digitized data into RAM
1	SelTC4	“1”	“1” = sum by 4; “0” = sum by 9
2	CmdSelEdge	“1”	“0” = select fall edge for fast command sampling (default)

3	NA	“1”	
4	Adc_TH<0>	“0”	Threshold corresponding to noise in ADC count
5	Adc_TH<1>	“0”	
6	Adc_TH<2>	“0”	
7	Adc_TH<3>	“0”	

Register # 1			
Bit	**Name**	**Default**	**Description**
0	MultFactor<0>	“1”	TOT vs ADC ratio for linearization (default ~25)
1	MultFactor<1>	“0”	
2	MultFactor<2>	“0”	
3	MultFactor<3>	“1”	
4	MultFactor<4>	“1”	
5	NA	“0”	
6	NA	“0”	
7	L1Offset<8>	“0”	L1 offset corresponding to L1 Latency

Register # 2			
Bit	**Name**	**Default**	**Description**
0	L1Offset<0>	“0”	L1 offset corresponding to L1 Latency
1	L1Offset<1>	“0”	
2	L1Offset<2>	“0”	
3	L1Offset<3>	“1”	
4	L1Offset<4>	“0”	
5	L1Offset<5>	“0”	
6	L1Offset<6>	“0”	
7	L1Offset<7>	“0”	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	IdleFrame<0>	“0”	Default 28 LSB “1100 --- 1100” of idle DAQ/T Frame
1	IdleFrame<1>	“0”	
2	IdleFrame<2>	“1”	
3	IdleFrame<3>	“1”	
4	IdleFrame<4>	“0”	
5	IdleFrame<5>	“0”	
6	IdleFrame<6>	“1”	
7	IdleFrame<7>	“1”	

Register # 4			
Bit	**Name**	**Default**	**Description**
0	IdleFrame<8>	“0”	Default 28 LSB “1100 --- 1100” of idle DAQ/T Frame
1	IdleFrame<9>	“0”	
2	IdleFrame<10>	“1”	
3	IdleFrame<11>	“1”	
4	IdleFrame<12>	“0”	
5	IdleFrame<13>	“0”	

6	IdleFrame<14>	“1”	
7	IdleFrame<15>	“1”	

Register # 5			
Bit	**Name**	**Default**	**Description**
0	IdleFrame<16>	“0”	Default 28 LSB “1100 --- 1100” of idle DAQ/T Frame
1	IdleFrame<17>	“0”	
2	IdleFrame<18>	“1”	
3	IdleFrame<19>	“1”	
4	IdleFrame<20>	“0”	
5	IdleFrame<21>	“0”	
6	IdleFrame<22>	“1”	
7	IdleFrame<23>	“1”	

Register # 6			
Bit	**Name**	**Default**	**Description**
0	IdleFrame<24>	“0”	Default 28 LSB “1100 --- 1100” of idle DAQ/T Frame
1	IdleFrame<25>	“0”	
2	IdleFrame<26>	“1”	
3	IdleFrame<27>	“1”	
4	ByPassCh0	“0”	!!! ONLY IN HG-V2A chip !!! Bypass trigger processing for debug purpose
5	ByPassCh17	“0”	
6	ByPassCh35	“0”	
7	NA	“0”	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	Tot_TH0<0>	“0”	TOT threshold used in TP (common to 9 channels)
1	Tot_TH0<1>	“0”	
2	Tot_TH0<2>	“0”	
3	Tot_TH0<3>	“0”	
4	Tot_TH0<4>	“0”	
5	Tot_TH0<5>	“0”	
6	Tot_TH0<6>	“0”	
7	Tot_TH0<7>	“0”	

Register # 8			
Bit	**Name**	**Default**	**Description**
0	Tot_TH1<0>	“0”	TOT threshold used in TP (common to 9 channels)
1	Tot_TH1<1>	“0”	
2	Tot_TH1<2>	“0”	
3	Tot_TH1<3>	“0”	
4	Tot_TH1<4>	“0”	
5	Tot_TH1<5>	“0”	
6	Tot_TH1<6>	“0”	
7	Tot_TH1<7>	“0”	

Register # 9			
Bit	**Name**	**Default**	**Description**
0	Tot_TH2<0>	“0”	TOT threshold used in TP (common to 9 channels)
1	Tot_TH2<1>	“0”	
2	Tot_TH2<2>	“0”	
3	Tot_TH2<3>	“0”	
4	Tot_TH2<4>	“0”	
5	Tot_TH2<5>	“0”	
6	Tot_TH2<6>	“0”	
7	Tot_TH2<7>	“0”	

Register # 10			
Bit	**Name**	**Default**	**Description**
0	Tot_TH3<0>	“0”	TOT threshold used in TP (common to 9 channels)
1	Tot_TH3<1>	“0”	
2	Tot_TH3<2>	“0”	
3	Tot_TH3<3>	“0”	
4	Tot_TH3<4>	“0”	
5	Tot_TH3<5>	“0”	
6	Tot_TH3<6>	“0”	
7	Tot_TH3<7>	“0”	

Register # 11			
Bit	**Name**	**Default**	**Description**
0	Tot_P0<0>	“0”	TOT pedestal used in TP (common to 9 channels)
1	Tot_P0<1>	“0”	
2	Tot_P0<2>	“0”	
3	Tot_P0<3>	“0”	
4	Tot_P0<4>	“0”	
5	Tot_P0<5>	“0”	
6	Tot_P0<6>	“0”	
7	NA	“0”	

Register # 12			
Bit	**Name**	**Default**	**Description**
0	Tot_P1<0>	“0”	TOT pedestal used in TP (common to 9 channels)
1	Tot_P1<1>	“0”	
2	Tot_P1<2>	“0”	
3	Tot_P1<3>	“0”	
4	Tot_P1<4>	“0”	
5	Tot_P1<5>	“0”	
6	Tot_P1<6>	“0”	
7	NA	“0”	

Register # 13			
Bit	**Name**	**Default**	**Description**
0	Tot_P2<0>	“0”	

1	Tot_P2<1>	“0”	TOT pedestal used in TP (common to 9 channels)
2	Tot_P2<2>	“0”	
3	Tot_P2<3>	“0”	
4	Tot_P2<4>	“0”	
5	Tot_P2<5>	“0”	
6	Tot_P2<6>	“0”	
7	NA	“0”	

Register # 14			
Bit	**Name**	**Default**	**Description**
0	Tot_P3<0>	“0”	TOT pedestal used in TP (common to 9 channels)
1	Tot_P3<1>	“0”	
2	Tot_P3<2>	“0”	
3	Tot_P3<3>	“0”	
4	Tot_P3<4>	“0”	
5	Tot_P3<5>	“0”	
6	Tot_P3<6>	“0”	
7	NA	“0”	

3.7 “Top sub-block” I2C parameters

Register # 0			
Bit	**Name**	**Default**	**Description**
0	EN_LOCK_CONTROL	“1”	Active the PLL lock detector : ‘0’ : OFF **‘1’ : ON : PLL lock detector activated**
1	ERROR_LIMIT_SC<0>	“0”	Configure the maximal error limit between EXT 40 MHz & PLL 40 MHz : ‘000’ : 0 difference ‘100’ : 1 difference … ‘111’ : 7 difference
2	ERROR_LIMIT_SC<1>	“1”	
3	ERROR_LIMIT_SC<2>	“0”	
4	Sel_PLL_Locked	“1”	Select the lock signal from PLL (“0”) or slow-control bit (“1”)
5	PllLockedSc	“1”	Slow-control lock pll signal
6	NA	“0”	
7	OrbitSync_sc	“0”	Slow-control OrbitSync signal

Register # 1			
Bit	**Name**	**Default**	**Description**
0	EN_PLL	“1”	Active the PLL to provide the different internal clks : ‘0’ : OFF : No clk “power off channels” **‘1’ : ON : PLL activated**
1	DIV_PLL_A	“0”	Choose the “OUT_CLK_SEL_READ” output frequency <A:B>: **'00' : 40 MHz** '10' : 160 MHz '01' : 320 MHz
2	DIV_PLL_B	“0”	

			'11' : 1280 MHz
3	EN_HIGH_CAPA	"0"	Add another large capacitor in the PLL LPF
4	EN_REF_BG	"1"	Activate the BANDGAP source 1V to the calibration part '0' : External PAD 'EXT_REF_TDC' **'1' : Internal 1V Bandgap 'BG_1V'**
5	VOUT_INIT_EN	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 2			
Bit	**Name**	**Default**	**Description**
0	VOUT_INIT_EXT_EN	"0"	Activate the DAC for V_PUMP_P voltage : '0' : external PAD "VOUT_INIT_EXT PLL" '1' : 5 bits DAC "VOUT_INIT_EXT_D<0:4>"
1	VOUT_INIT_EXT_D<0>	"0"	5 bits DAC for VOUT_INIT PLL voltage : '00000' = 0 V '11111' = 1.2 V
2	VOUT_INIT_EXT_D<1>	"0"	
3	VOUT_INIT_EXT_D<2>	"0"	
4	VOUT_INIT_EXT_D<3>	"0"	
5	VOUT_INIT_EXT_D<4>	"0"	
6	NA	"0"	
7	NA	"0"	

Register # 3			
Bit	**Name**	**Default**	**Description**
0	FOLLOWER_PLL_EN	"1"	Activate the VTC for the bias PLL bias (pump charge injection): '0' : OFF **'1' : VTC 6 bits "BIAS_I_PLL_D<0:5>**
1	BIAS_I_PLL_D<0>	"0"	Configure the VTC the bias PLL BIAS_N_PLL bias (pump charge injection current) : Current = DATA<0:5> Weight addition (**default 30 µA**)
2	BIAS_I_PLL_D<1>	"0"	
3	BIAS_I_PLL_D<2>	"0"	
4	BIAS_I_PLL_D<3>	"1"	
5	BIAS_I_PLL_D<4>	"1"	
6	BIAS_I_PLL_D<5>	"0"	
7	Sel_40M_ext	"0"	"1" = select the external 40MHz clock

Register # 4			
Bit	**Name**	**Default**	**Description**
0	EN1_probe_pll	"1"	Current value of the CLPS driver dedicated to probe the PLL
1	EN2_probe_pll	"1"	
2	EN2_probe_pll	"0"	
3	EN-pE0_probe_pll	"0"	Current value of the CLPS pre-emphasis driver dedicated to probe the PLL
4	EN-pE1_probe_pll	"0"	
5	EN_pE2_probe_pll	"0"	
6	S0_probe_pll	"0"	Delay value of the CLPS pre-emphasis driver dedicated to probe the PLL
7	S1_probe_pll	"0"	

Register # 5			
Bit	**Name**	**Default**	**Description**
0	EN1	"1"	

1	EN2	“1”	Current value of the CLPS drivers (Data/Trigger)
2	EN3	“0”	
3	EN-pE0	“0”	Current value of the CLPS pre-emphasis driver (Data/Trigger)
4	EN-pE1	“0”	
5	EN-pE2	“0”	
6	S0	“0”	Delay value of the CLPS pre-emphasis driver (Data/Trigger)
7	S1	“0”	

Register # 6			
Bit	**Name**	**Default**	**Description**
0	Sel_ReSync_fcmd	“1”	“0” = select external ReSync signal
1	Sel_L1_fcmd	“1”	“0” = select external L1 signal
2	Sel_STROBE_fcmd	“1”	“0” = select external strobe signal
3	Sel_OrbitSync_fcmd	“1”	“0” = select external OrbitSync signal
4	NA	“0”	
5	NA	“0”	
6	NA	“0”	
7	NA	“0”	

Register # 7			
Bit	**Name**	**Default**	**Description**
0	En_PhaseShift	“1”	“1” = enable the PhaseShifter
1	Phase<0>	“0”	Phase shift value
2	Phase<1>	“0”	
3	Phase<2>	“0”	
4	Phase<3>	“0”	
5	NA	“0”	
6	NA	“0”	
7	En_pll_ext	“0”	